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Digital Implementation of a Novel Controlled Rectifier Synchronization Method

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Synchronization of a control signal with grid voltage on the basis of zero crossing is not convenient in digital control systems because of disturbances causing multi-crossing of zero and additional hardware required for detection. A new method of synchronization to AC networks for phase-controlled rectifiers or for front-end rectifiers is presented in this article. All theoretical dependencies are also included.

Keywords AC/DC converters, active filters, DSP, FPGA

1. Introduction

Phase synchronization is a very significant problem in many power converters connected to the grid. Properties of the phase synchronization algorithm are dependent on the voltage quality in a grid. As a result of many power electronics converters connected to the grid, the quality of voltage is rather low. Higher voltage harmonics, voltage sags

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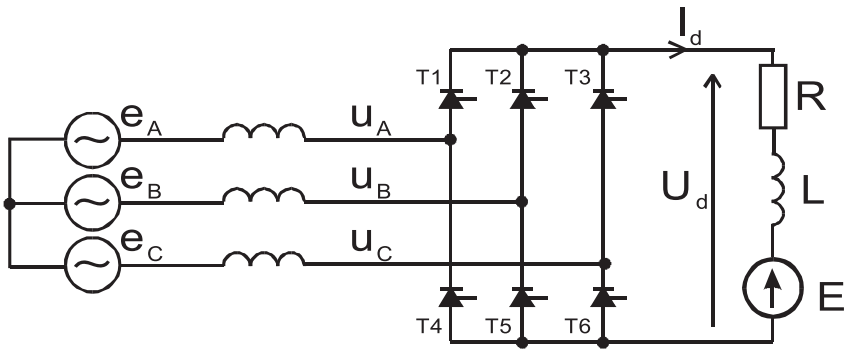

Figure 1. Phase controlled rectifier.

and especially autonomous grid frequency variations are serious problems for phase synchronization algorithms. Low quality phase synchronization can also influence converter operation. Previously, that problem was connected mainly with phase-controlled rectifiers (Figure 1). Currently the main focus of synchronization is in the realization of fully controlled rectifiers with transistors widely used in motion AC/DC/AC converters, active filters and UPS systems [1–4]. Typical power electronics converters, which require phase synchronization, are presented in Figures 1 and 2.

In many converters, synchronization between grid voltage and switching control signals is necessary [5, 6]. The simplest way is to determine instants when voltage is crossing zero [7]. In the modern converters, that simplest method cannot be used directly because of disturbances in the grid [8]. Those effects are caused by the presence of many converters with power electronic elements. In the voltage waveform, multiple zero crossing instants can appear, which can cause inappropriate operation of synchronization circuits.

A better solution is to add analogue or digital phase locked loop circuits [9]. Unfortunately, use of common PLL circuits will not guarantee good results. In a grid with a high disturbance level, PLL circuits can work incorrectly. Different proposals of PLL modifications, which can improve PLL properties, were presented in [5, 10–15]. Such modifications are sometimes very complex and require complicated practical realization of the system.

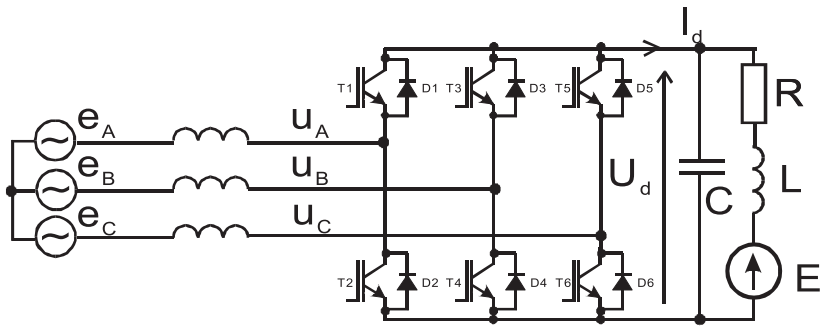

Figure 2. Fully controlled rectifier.

On the other hand, it is possible to realize a synchronization system with better properties and with possibility of simple realization in the real system. A method, which uses simple trigonometric dependencies, is presented in this article.

2. Synchronization Method

In conventional converters, which use a PLL, the measured grid voltage signal is used to find the zero crossing. Grid voltage is introduced to the synchronization block directly or after using a low pass filter. Such a system is sensitive to distortions of sinusoidal waveforms where a few zero crossings occur. In the presented method, instead of zero crossing checking, a calculation of actual grid voltage phase angle is proposed.

Phase Angle Calculation

Calculations of actual phase angle are provided with sampling time specified by angle φ proportional to actual grid voltage period. Notations used for equations are shown in Figure 3.

Measured samples of voltages in consecutive instants are defined as follows:

$$u_{k-2} = U \sin(\alpha_{k-1} - \varphi), \tag{1}$$

$$u_{k-1} = U \sin(\alpha_{k-1}), \tag{2}$$

$$u_k = U \sin(\alpha_{k-1} + \varphi), \tag{3}$$

where φ is the phase angle between consecutive measurements and α_{k-1} is the angle at instant $k-1$; u_{k-2}, u_{k-1}, u_k, are samples of grid voltage, U is the magnitude of grid voltage.

When magnitude U is eliminated from Eqs. (1), (2) and from (2), (3) the next dependencies are obtained:

$$u_{k-2} \sin(\alpha_{k-1}) = u_{k-1} \sin(\alpha_{k-1} - \varphi), \tag{4}$$

$$u_k \sin(\alpha_{k-1}) = u_{k-1} \sin(\alpha_{k-1} + \varphi). \tag{5}$$

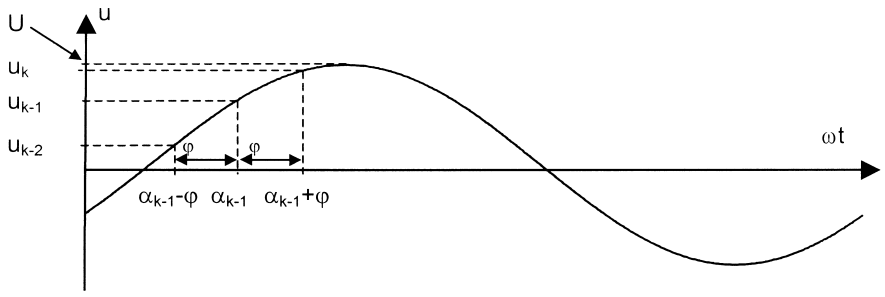

Figure 3. Notation of phase angles.

Using trigonometric dependencies for sine of sum and difference of two angles, the next equations are derived:

$$u_{k-1}\sin(\alpha_{k-1})\cos(\varphi) = u_{k-1}\cos(\alpha_{k-1})\sin(\varphi) - u_{k-2}\sin(\alpha_{k-1}) = 0, \tag{6}$$

$$u_{k-1}\sin(\alpha_{k-1})\cos(\varphi) + u_{k-1}\cos(\alpha_{k-1})\sin(\varphi) - u_k\sin(\alpha_{k-1}) = 0. \tag{7}$$

Assuming that angle φ is less than 0.5π the trigonometric functions for the angle φ are specified from (6) and (7):

$$\cos(\varphi) = \frac{u_{k-2} + u_k}{2u_{k-1}}, \tag{8}$$

$$\sin(\varphi) = \frac{u_{k-2} - u_k}{2u_{k-1}}\tan(\alpha_{k-1}). \tag{9}$$

Calculation of the angle φ using arc cosine function for (8) is necessary if AC grid frequency is not exactly known. A quartz oscillator and digital counter guarantee constant sampling time.

The function tangent of the angle α_{k-1} is dependent on φ:

$$\tan(\alpha_{k-1}) = \frac{u_{k-1}\sin(\varphi)}{u_{k-1}\cos(\varphi) - u_{k-2}}. \tag{10}$$

The angle α_{k-1} is calculated as follows:

$$\alpha_{k-1} = \arctan\left(\frac{u_{k-1}\sin(\varphi)}{u_{k-1}\cos(\varphi) - u_{k-2}}\right). \tag{11}$$

The angle α_k in instant k is defined:

$$\alpha_k = \alpha_{k-1} + \varphi. \tag{12}$$

If the voltage u_k is less than zero, then the angle α_k is increased by π. During calculation all limits of calculation are controlled. If some limits are exceeded, then α_{k-1} is calculated from the following dependence:

$$\alpha_{k-1} = \alpha_{k-2} + \varphi. \tag{13}$$

The calculated value of angle α_k denoted as α_{cal} was used as the input for PLL circuit.

In the proposed synchronization method, a high sampling frequency is not needed. Only a few samples for grid voltage period is sufficient, for example 12 samples for 20 (ms), a grid voltage period that corresponds to angle φ equal to 30 (deg). As investigation shows, for values of φ less than 10 (deg), problems connected with small differences between samples of grid voltages can appear. In such cases, errors of angle calculation from (11) are too large because the denominator is near zero.

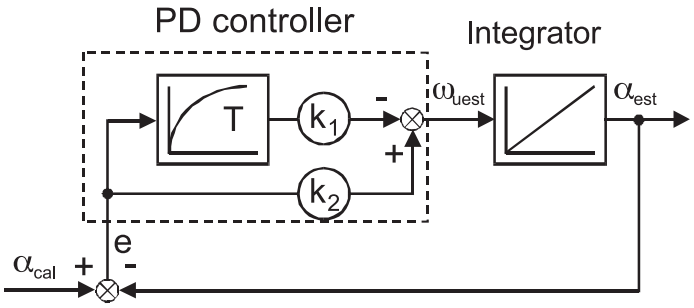

Figure 4. Phase locked loop.

Phase Locked Loop

The phase locked loop used in the synchronization process is presented in Figure 4.

The PLL circuits consist of a PD controller and integrating system. The task of the PD controller is to set estimated grid voltage pulsation to the level, which ensures minimization of error between calculated α_{cal} and estimated α_{est} angle. The PD controller is described using dependence:

$$\omega_{uest}(t) = k_2 e(t) + \frac{k_1}{T}\frac{de(t)}{dt}. \tag{14}$$

Coefficients of the PD controller: k_1, k_2, and T have principal influence on dynamical properties of the PLL loop. In the presented system, coefficients were tuned experimentally by trial and error method in a simulation program. Tuning of the PD controller should be provided in such a manner that guarantees that coefficient k_2 is greater than k_1. Simulations and experiments used coefficients with values presented in Table 1.

Full Synchronization System

The full synchronization system for a single-phase circuit is presented in Figure 5.

Grid voltage $u(t)$ is measured and converted using an A/D converter sampled with period $T_{SAMPLING}$. Measured samples of grid voltage are used in phase angle calculations, which are provided with calculation period T_{CALCUL}.

In the PLL part of the system, calculated angle α_{cal} is compared with estimated angle α_{est} using a PD controller that tunes the estimated pulsation of grid voltage ω_{uest}.

In a digital system, instants of calculation of phase angle should be identical to instants of measurements of grid voltage with regards to the A/D conversion time. Another simpler solution is to use an A/D converter with high sampling frequency to make a digital

Table 1
Coefficients of phase locked loop

Coefficient	Value
T	3 (ms)
k_1	0.25 (—)
k_2	0.5 (—)

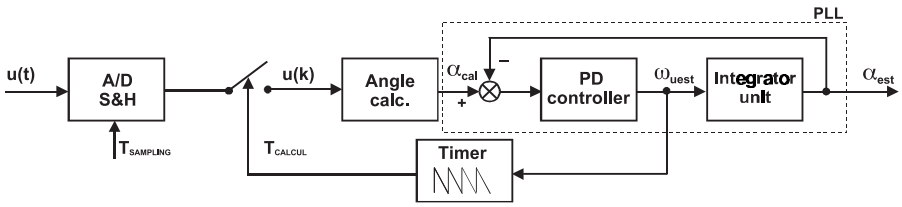

Figure 5. Synchronization diagram.

measurement system closer to the analog one. Good results were obtained for an A/D converter sampled with 50 [μs] period for 50 [Hz] grid voltage.

3. Simulation Results

Simulation investigations were prepared using software written in C language. In a simulation program the system consists of a three-phase grid, line inductance, 6-pulse-thyristor rectifier and an RL load (Figure 6). All variables presented are in per unit.

The measured grid voltage signal was distorted using an additional random waveform and some fault zero voltage measurement. Example of the distorted signal is presented in Figure 7.

Start up of the synchronization method, which shows the tuning process to the grid voltage frequency, is presented in Figure 8 for a distorted and non-distorted voltage. In spite of incorrect measurements, the synchronization system is tuned to the grid voltage of 50 Hz frequency in less than 1 s with an error smaller than 2.5%.

Operation of the proposed system during step change of grid voltage frequency from 45 Hz to 55 Hz is presented in Figure 9. On the basis of transients presented in Figure 9, it is possible to notice that the presented system has good properties in the selected range of frequencies.

Operation of the system in the presence of a high constant offset in measured grid voltage is presented in Figure 10. The proposed synchronization method is totally insensitive to the presence of constant offset. Frequency error in steady state is less than 2.5%. Such a feature could be very convenient in the system where AD converter with unipolar inputs is used.

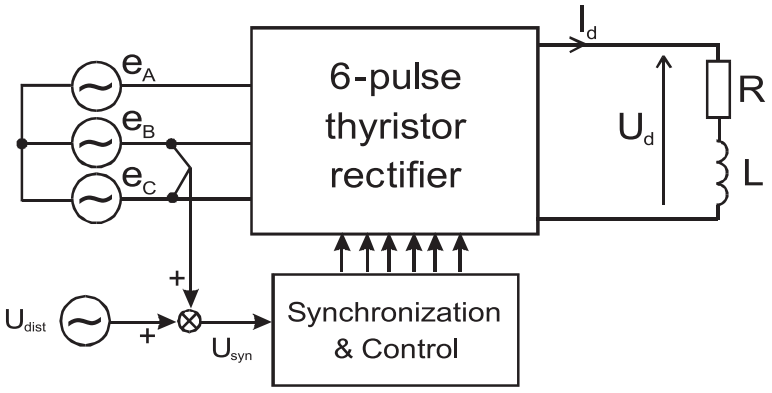

Figure 6. Rectifier with proposed synchronization control.

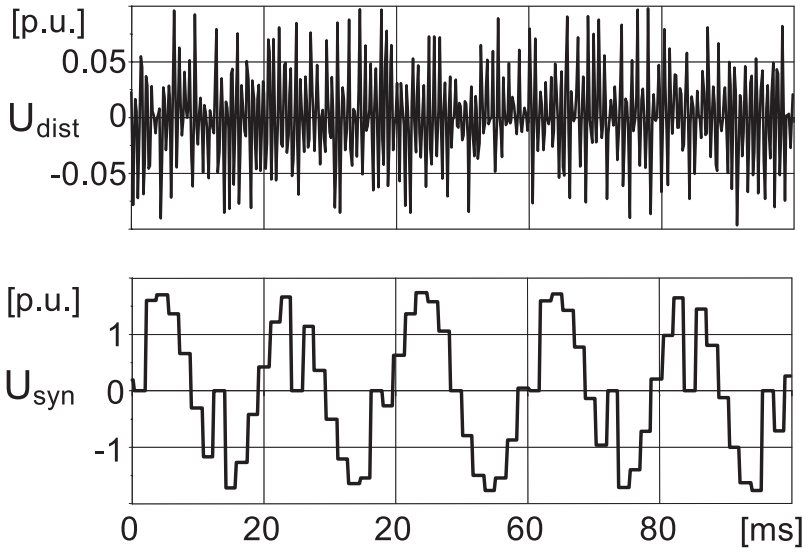

Figure 7. Network voltage with incorrect measurements and notch-type disturbance.

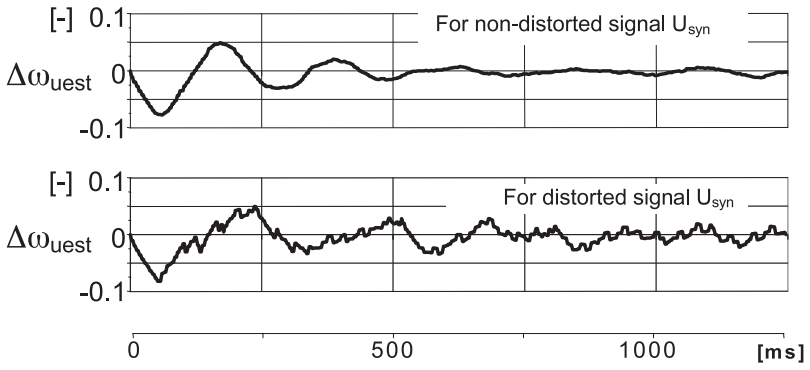

Figure 8. Start up of the synchronization method.

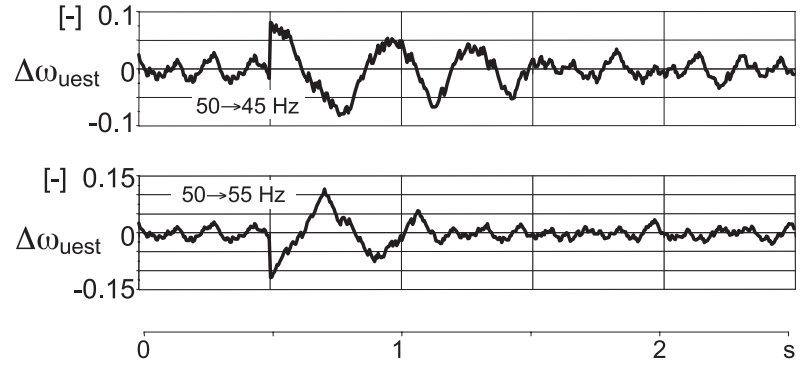

Figure 9. Step change of grid voltage frequency from 45 Hz to 55 Hz.

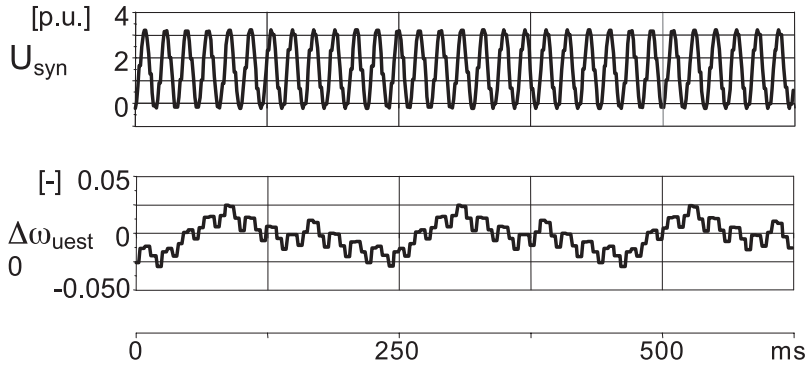

Figure 10. Operating with presence of high level constant offset in measured voltage.

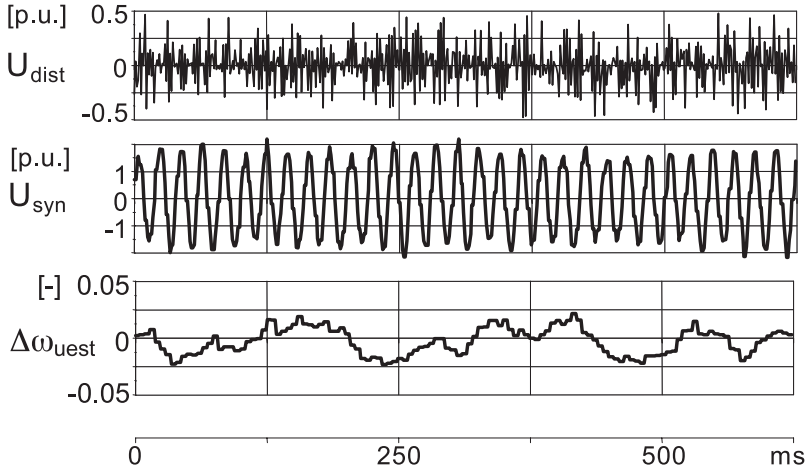

Figure 11. Operation of the synchronization system with high level of higher voltage harmonics.

Operation of the synchronization system with a high level of random higher order harmonics is presented in Figure 11. The performance of the synchronization method was also analyzed on the criteria of phase shift response (Figures 12 and 13). With a simulation time of 50 (ms), the grid voltage vector makes a positive (Figure 12) and negative (Figure 13) phase shift step of 12°. Using proposed algorithm phase shift is estimated in a 150 (ms) time with a small overshoot (Figure 12). In Figure 13, there is no overshoot in the estimated phase shift.

4. Implementation and Experimental Results

The synchronization method presented in this article was implemented in a laboratory 3-phase converter. A thyristored rectifier feeding a 5.5 kW separately excited DC motor was used in the experiments. The rectifier was powered from a typical 3×380 (V) 50 (Hz) grid.

A control board SH65L was used in the control system of the investigated drive. The control board SH65L, designed and made in Gdansk University of Technology,

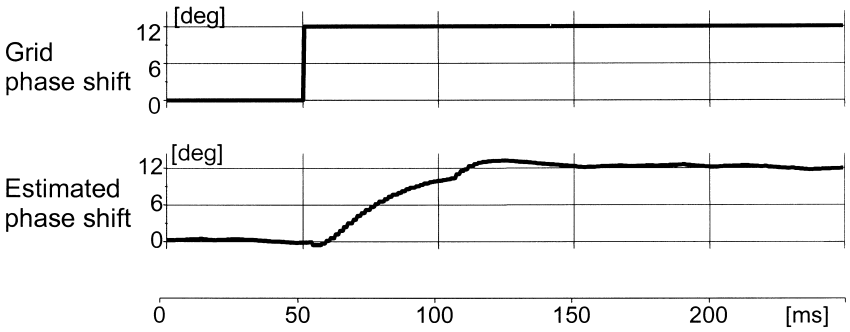

Figure 12. Estimated phase shift response to a grid phase shift.

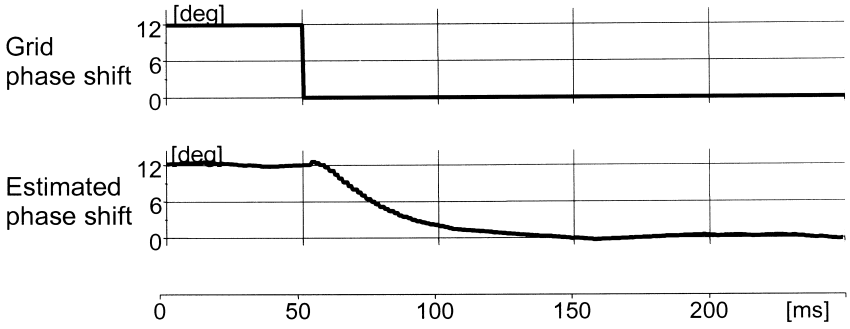

Figure 13. Estimated phase shift response to a grid phase shift.

consists of floating-point digital signal processor ADSP21065L and field programmable gate arrays (FPGA) circuit FLEX6000 (Figure 14). The control board was connected to the PC computer using a RS232C interface. Connection to PC allows bidirectional communication with the control board. It is easy to run, monitor, and acquire data using the control panel program written in C++ Builder. Control software was written in C language using ADSP21000 C library. Open-source software can be easily changed.

An example of the line-to-line voltage waveform in a laboratory electrical grid is presented in Figure 15. The waveform was saved using digital signal oscilloscope. The voltage waveform presented in Figure 15 shows the laboratory voltage where the proposed synchronization method was tested. Simultaneously, with the tested converter, other inverters and rectifiers were working.

The investigated rectifier, which scheme was presented in Figure 6, was properly synchronized with grid voltage. Other older converters, accessible in laboratory, with simple zero crossing synchronization control had occasional problems with synchronization.

The presented system works properly in transients, as shown in Figure 16. The measured output voltage U_d and the output current I_d pulses of the rectifier in Figure 6 have stable shape.

The measured grid voltage in a laboratory system was also additionally distorted. In the regular time instant, the measured voltage was set to zero. The results obtained for distorted voltage are presented in Figure 17.

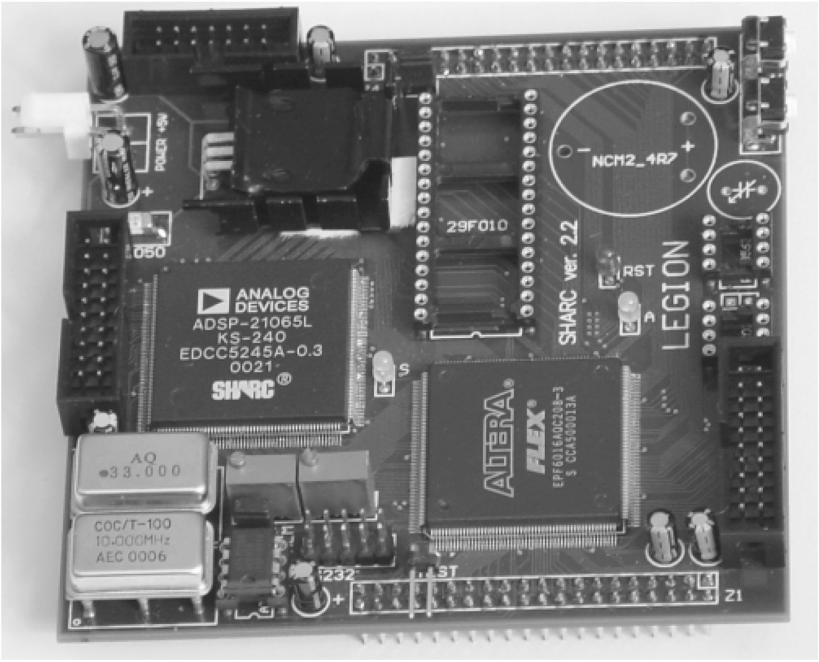

Figure 14. SH65L control board with ADSP21065L and FLEX 6000 circuits.

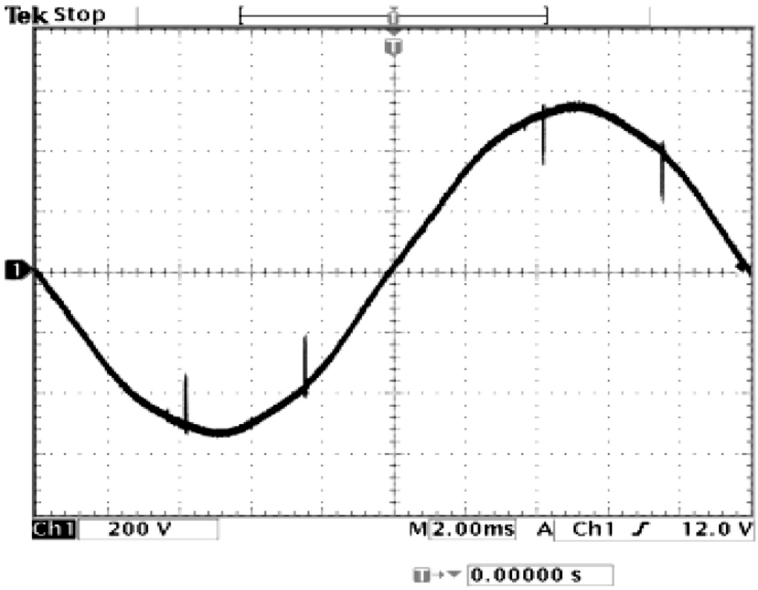

Figure 15. Waveform of laboratory grid voltage.

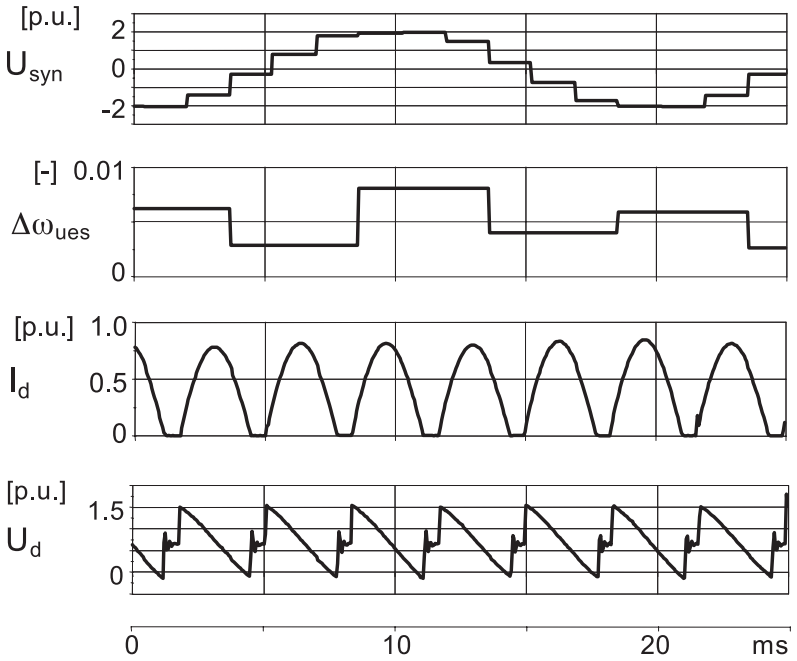

Figure 16. Operation of rectifier–measured values in steady-state.

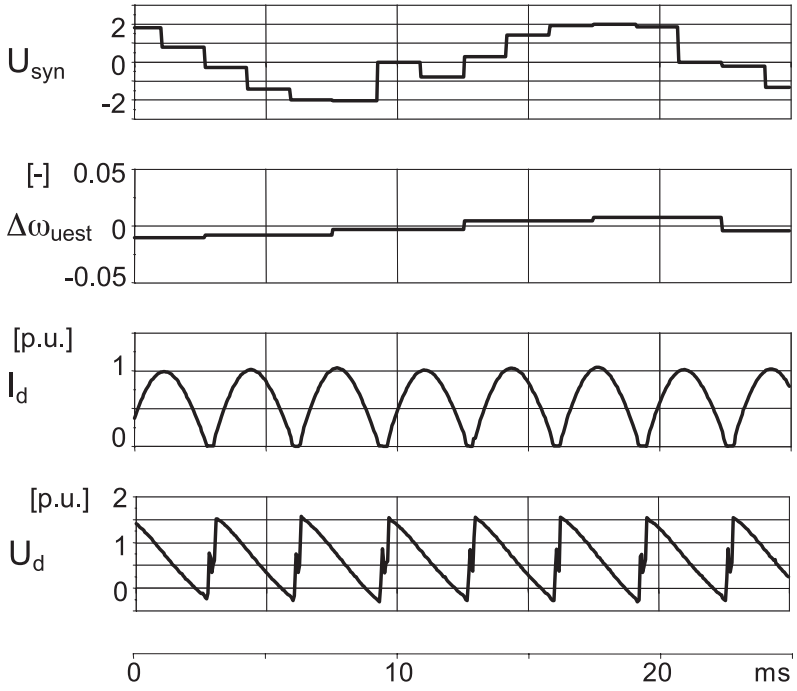

Figure 17. Operation of rectifier with additionally distorted grid voltage.

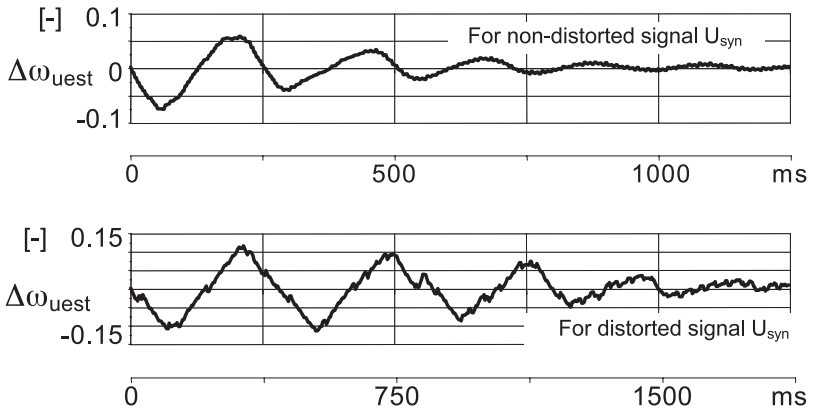

Figure 18. Waveforms of error of estimated grid frequency during start up of the system.

Waveforms of error in estimated grid frequency during start up of the system are presented in Figure 18. In Figure 18, waveforms are presented for suitable non-distorted and distorted grid voltage signal.

The obtained experimental results fully confirm correctness and good properties of the proposed synchronization method. Starting time of the system is short and less than 1.5 s for distorted signals. For non-distorted signals, the results are much better.

The synchronization system with coefficients $k_1 = 0.25$, $k_2 = 0.5$, and $1/T = 0.3$ was used in a laboratory tests. The same coefficients were used in simulation program. Coefficients values were chosen using observation of a series of experimental results. In the future, calculation of the coefficients should be considered.

5. Conclusions

The results obtained from simulations and experiments confirm that the proposed synchronization method is very proper. The presented method could be used in control systems of presently much more popular grid inverters.

The proposed synchronization method assures fast synchronization time. Disturbances appearing in the grid have no practical influence on operation of the system. Simple setting of coefficients and a simple algorithm facilitate the practical realization of the proposed synchronization method.

References

1. Z. Benčić, Z. Jakopović, and V. Šunde, "An integral view of AC/DC rectifiers and current-source inverters based on single phase bridge," *EPE-PEMC*, Dubrovnik, Croatia, 2002.
2. J. M. Carrasco, E. Galvan, G. Escobar, and A. M. Stankovic, "Passivity–based controller for a three phase synchronous rectifier," *IECON*, Nagoya, Japan, 2000.
3. N. A. Losic, L. Cheng, and V. Khatri, "Modeling and design of a vector-controlled PWM active rectifier," *IECON*, Denver, USA, 2001.
4. M. Malinowski and M. P. Kaźmierkowski, "A comparative study of control techniques for PWM rectifiers in AC adjustable speed drives," *IECON*, Denver, USA, 2001.
5. B. Tamyurek and D. A. Torrey, "A high power-quality, three-phase utility interface," *APEC*, Dallas, USA, 2002.

6. G. Zhemerov, N. Ilyna, and D. Krylov, "A novel near unity power factor converter system based on compensated controlled rectifier," *EPE-PEMC*, Dubrovnik, Croatia, 2002.
7. R. Weindenbrug, F. P. Dawson, and E. Bonert, "New synchronization method for thyristor power converters to weak AC-systems," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 5, pp. 505–511, October 1993.
8. M. H. J. Bollen, "Fast assessment method for voltage sags in distribution systems," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1414–1423, November/December 1996.
9. G. C. Hsieh and J. C. Hung, "Phase-locked loop techniques—A survey," *IEEE Transactions on Industrial Electronics*, vol. 43, no. 6, pp. 609–615, December 1996.
10. S. Pavljašević and F. Dawson, "Phase synchronization using zero crossing sampling digital phase-locked loop," *PCC-Osaka*, Japan, pp. 665–670, 2002.
11. S. Pavljašević and F. Dawson, "Synchronization to utility network signals containing a high level of disturbances," *PCC-Osaka*, Japan, pp. 1050–1055, 2002.
12. A. A. El-Amawy and A. Mirbod, "An efficient software controlled PLL for low frequency application," *IEEE Transactions on Industrial Electronics*, vol. 35, no. 2, pp. 341–344, May 1988.
13. O. Vainio and S. J. Ovaska, "Noise reduction in zero crossing detection by predictive digital filtering," *IEEE Transactions on Industry Applications*, vol. 42, no. 1, pp. 55–62, February 1995.
14. A. A. Girgis, W. B. Chang, and E. B. Makram, "A digital recursive measurement scheme for on-line tracking of power system harmonics," *IEEE Transactions on Power Delivery*, vol. 6, no. 3, pp. 1153–1160, July 1991.
15. Y. V. Murty and W. J. Smolinski, "A Kalman filter based digital percentage differential and ground fault relay for a 3-phase power transformer," *IEEE Transactions on Power Delivery*, vol. 5, no. 3, pp. 1299–1306, July 1990.