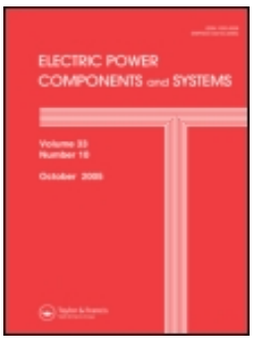

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Problems of Exact Generation of Inverter Output Voltage

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In this work, a new voltage space vector PWM method is developed. The problem of exact generation of small voltage vectors is discussed. Two methods for generating small inverter output voltage vectors are proposed. The influence of dead time is explained and its effect on the motor current is compensated. A squirrel cage induction motor with reduced supply voltage is used for testing the developed algorithm. Simulation and experimental results are carried out using fixed-point (DSP) and (FPGA). In addition, the practical realization of the proposed algorithm is discussed.

Keywords PWM, voltage source inverter, voltage space vector, dead time, DSP, FPGA

1. Introduction

The most popular method of induction motor speed control is to change the amplitude and frequency of the applied voltage. In an ac motor vector control,

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the fundamental harmonic of the inverter output voltage produces the main effect on the motor operation. This component is a function of the control system used. Any deviations of this voltage from the reference value have an effect on the drive performance. These deviations are caused by the introduction of a dead time in the inverter control algorithm and the required minimum switching time. The compensation principle of the dead-time effect is well known and is used in many systems [6, 7, 9, 10].

In advanced motor drive systems, a control signal is most often used in the form of stator current amplitude and its angular frequency. Such control methods make the voltage inverter a current source and make it possible to design drive systems with the best dynamic. This is because of the direct relation between the stator current and developed torque [2, 3]. In most cases, the implemented current control is similar in action to analog hysteresis controllers. The advantage of such a solution is the simplicity of the system, which is obtained at the cost of control quality. Hysteresis controllers require high frequency switching transistors, which affect the loss and efficiency of the drive system. In [5], a digital algorithm is presented for hysteresis stator current control. The modified switching sectors make it possible to obtain the controlled current in the desired zone, which simultaneously protects the system before an unnecessary increase in the switching frequency.

Predictive current controllers provide satisfactory results, especially with fixed switching frequency [4, 7, 8, 11, 13]. Many publications denote the need for a current control system that is not sensitive to changing parameters of the controlled object and provides information about the first order of the voltage waveform without delay.

Inverter output voltage generation using the space vector Pulse Width Modulation (PWM) method requires a fast microprocessor to realize the sophisticated calculations. Technical operating conditions of a microprocessor lead to certain limitations in determining the switching instants. During practical implementation, the appearance of additional problems make simple PWM algorithm implementation more elaborate. With the introduction of novel power electronics switches, such as Insulated Gate Bipolar Transistor (IGBTs), it was possible to design converters with high switching frequencies. The increase in switching frequency, and introducing the necessary dead time, which is required to correct the inverter operation, provide a distortion of the output current and voltage waveforms.

In this work, the voltage space vector PWM method is realized. The effect of dead time has been compensated using the developed method. For full use of the output voltage (without providing over modulation), a squirrel cage induction motor with reduced line voltage 300 [V] is used.

The increased use of Programmable Logic Devices (PLD) and Field Programmable Gate Array (FPGA) systems result from their advantages: short time for developing prototypes and easy modification. The main significance of PLD/FPGA systems is that they have intelligent and convenient Computer Aided Design (CAD) systems, replacing microprocessor control systems and designed to the form of higher order computer programming. The use of FPGA systems makes it possible to realize parts of the control system by using hardware that frees the main processor from parts of the realized tasks. In this article, experimental results for the control system are realized on DSP TMS320C50 and partly on FPGA systems (FLEX6000 family).

2. Maximum Inverter Output Voltage

The inverter output voltage is delivered from an uncontrolled three-phase diode rectifier, and its average value for the 380 V bus is [12]

$$U_d = U_{RS} \cdot \sqrt{2} \cdot \frac{3}{\pi} = 380 \cdot \sqrt{2} \cdot \frac{3}{\pi} = 513.2 \text{ V} \tag{1}$$

Due to the capacitors in the dc bus, in the case of low inverter load, the voltage in the intermediate dc bus may reach a maximum voltage value of

$$U_{d\max} = U_{RS} \cdot \sqrt{2} = 380 \cdot \sqrt{2} = 537.4 \text{ V} \tag{2}$$

Therefore the voltage in the dc bus, depending on the inductive load and capacitance may change from 513 V to 537 V (5% change). If we measure the motor phase voltage in reference to the midpoint of the dc bus capacitors, each motor phase is connected to the voltage $+U_d/2$ or $-U_d/2$. The transformation factor a_{tr} could be defined as

$$a_{tr} = \frac{\sqrt{2} \cdot U_{RS}}{\sqrt{3} \cdot \frac{U_d}{2}} \tag{3}$$

From (3), the inverter line output voltages is

$$U_{UV} = a_{tr} 0.827 U_{RS} \tag{4}$$

The maximum inverter output voltage may be achieved with rectangular output waveforms if the switches alternate every 180°. In this case, on the basis of harmonic analysis of the above waveform, the following can be calculated:

$$a_{tr} = \frac{4}{\pi} = 1.27 \tag{5}$$

where the inverter output voltage is

$$U_{UV} = 1.27\ 0.827 U_{RS} = 1.05 U_{RS} \tag{6}$$

which is 5% higher than the rectifier input voltage.

In the case of sinusoidal PWM, when the sinusoidal modulated waveform is compared with the carrier waveform, the factor a_{tr} assumed generally to be unity value and the inverter output line voltage is given by

$$U_{UV} = 0.827 U_{RS} \tag{7}$$

We can note that the system does not use the full 380 V supply voltage, because, at the inverter output, only about 314 V is obtained. This limits the maximum output frequency in the vector control method.

3. Voltage Space Vector PWM

The output voltage is described using the actual state of the inverter switches. There are eight positions of inverter switches, six active and two zero vectors, shown

in Figure 1. PWM voltage space vector methods are based on the representation of three phase quantities using a vector described in a two-dimensional space coordinate system, α–β. The system of three sinusoidal voltages changing in time is modeled using space vector, with amplitude U_{om}, rotating on the stationary α–β plane with angular speed ω_o.

The commanded output voltage $U_o(\omega_o t)$ is obtained using a combination of inverter output vectors U_{vi} $(i = 0 \cdots 7)$. A minimum switching number during the generation process of voltage vector, $U_o(\omega_o t)$, is obtained by using directly adjacent vectors U_{vi}. These vectors make the next sequence: z_1-n_1-n_2-z_2-n_2-n_1-z_1, where: z_i is the zero vector ($i = 0$ or 7) and n_i is the active vector $(i = 1 \cdots 6)$. Switching combinations of inverter transistors, which correspond to the vectors of the above sequence, differ from each other only by the state of one switch. The active voltage is obtained from three-phase to two-phase transformation and is given by

$$U_v = \sqrt{\frac{2}{3}} U_d, \tag{8}$$

where U_d is the inverter input voltage.

Using vector representation shown in Figure 2, the output voltage vector U_o may be described as:

$$\overline{U}_o = \frac{t_1}{T_{imp}} \overline{U}_{vi} + \frac{t_2}{T_{imp}} \overline{U}_{v(i+1)} \tag{9}$$

where $i = 1 \cdots 6$.

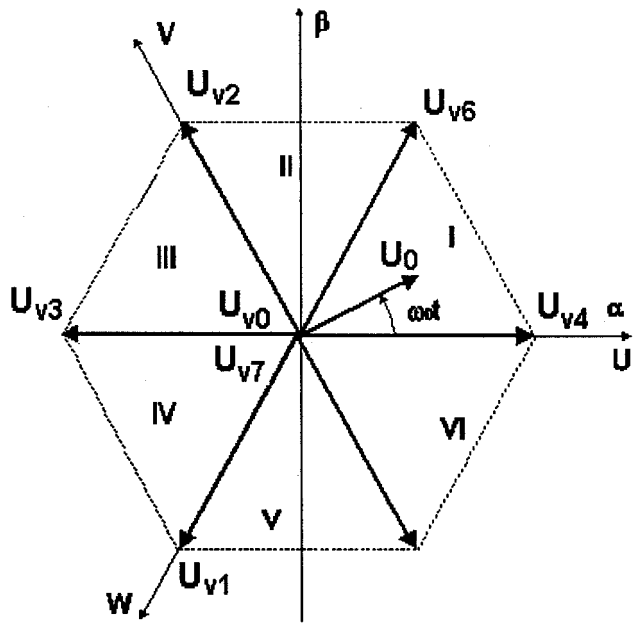

Figure 1. The position of output voltage space vectors for the states of switches.

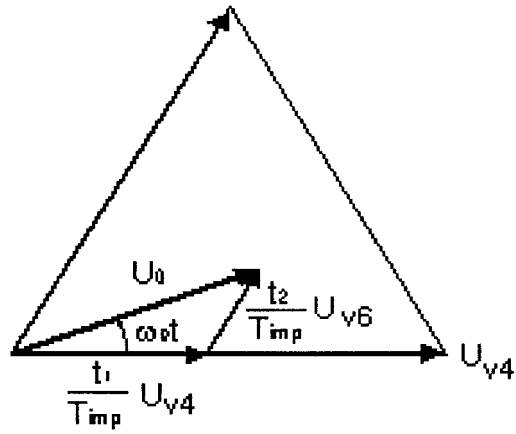

Figure 2. Identification of duration time for first sector of the inverter switches.

Using (9) the vector components in an α–β system are

$$U_{o\alpha} = \frac{t_1}{T_{imp}} U_{vi\alpha} + \frac{t_2}{T_{imp}} U_{v(i+1)\alpha}, \tag{10}$$

$$U_{o\beta} = \frac{t_1}{T_{imp}} V_{vi\beta} + \frac{t_2}{T_{imp}} U_{v(i+1)\beta}. \tag{11}$$

From above, the switching time of active vectors may be calculated from

$$t_1 = T_{imp} \frac{U_{o\alpha} \cdot U_{v(i+1)\beta} - U_{o\beta} \cdot U_{v(i+1)\alpha}}{U_{vi\alpha} \cdot U_{v(i+1)\beta} - U_{vi\beta} \cdot U_{v(i+1)\alpha}}, \tag{12}$$

$$t_2 = T_{imp} \frac{-U_{o\alpha} \cdot U_{vi\beta} + U_{o\beta} \cdot U_{vi\alpha}}{U_{vi\alpha} \cdot U_{v(i+1)\beta} - U_{vi\beta} \cdot U_{v(i+1)\alpha}}, \tag{13}$$

$$t_0 = T_{imp} - t_1 - t_2. \tag{14}$$

In [5], two methods of calculating the times t_1, t_2, and t_o, in the cycle z_1-n_1-n_2-z_2-n_2-n_1-z_1, are presented as follows:

- Times t_1, t_2, and t_o are calculated for each half cycle separately (for z_1-n_1-n_2-z_2 and after that for z_2-n_2-n_1-z_1).
- Times t_1, t_2, and t_o are calculated for the first half cycle z_1-n_1-n_2-z_2 and after that the same times are used in the next sequence, z_2-n_2-n_1-z_1.

Generally, it is assumed that the switching period T_{imp} is the time of all sequence z_1-n_1-n_2-z_2-n_2-n_1-z_1 [8]. In this work, similar to [1], the sequence z_1-n_1-n_2-z_2-n_2-n_1-z_1 lasts for two periods T_{imp}, as seen in Figure 3.

In Table 1, the sequence of vectors switching for each sector is shown. In the literature, two types of vector number notations are used.

1. Active vectors in voltage hexagonal are numbered as follows: 1, 2, 3, 4, 5, 6
2. Active vectors are denoted by numbers, which correspond to binary combination of transistor states as 4, 6, 2, 3, 1, 5.

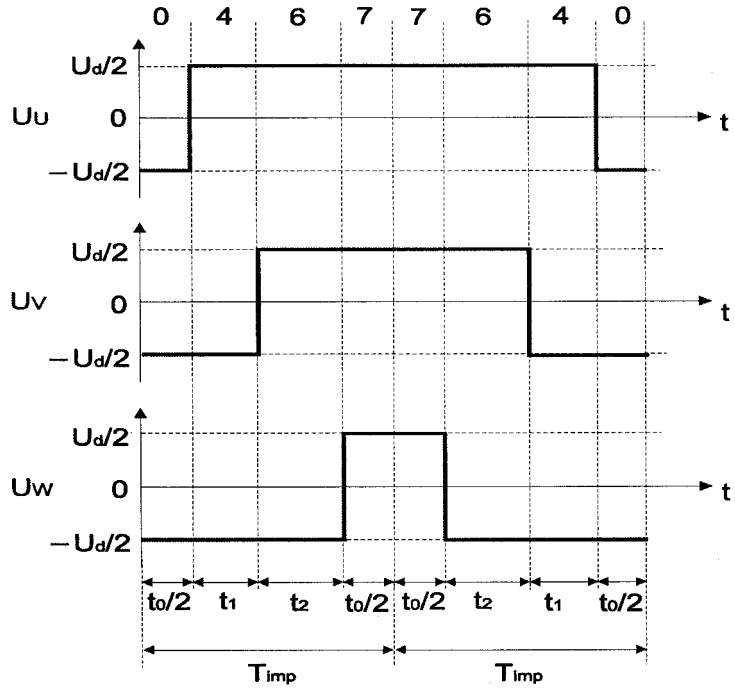

Figure 3. Inverter output voltages for the three phases in sector I.

Table 1
Vector switching sequences

Sector	z_1	n_1	n_2	z_2	n_2	n_1	z_1
I	U_{v0}	U_{v4}	U_{v6}	U_{v7}	U_{v6}	U_{v4}	U_{v0}
II	U_{v7}	U_{v6}	U_{v2}	U_{v0}	U_{v2}	U_{v6}	U_{v7}
III	U_{v0}	U_{v2}	U_{v3}	U_{v7}	U_{v3}	U_{v2}	U_{v0}
IV	U_{v7}	U_{v3}	U_{v1}	U_{v0}	U_{v1}	U_{v3}	U_{v7}
V	U_{v0}	U_{v1}	U_{v5}	U_{v7}	U_{v5}	U_{v1}	U_{v0}
VI	U_{v7}	U_{v5}	U_{v4}	U_{v0}	U_{v4}	U_{v5}	U_{v7}

In this work, the second notation is used by numbering the output voltage vectors as the sequence 0, 4, 6, 3, 1, 5, 7.

4. The Effect of the Dead-Time on the Drive System Operation

With the introduction of novel power electronics switches like IGBTs, it was possible to design converters with high switching frequencies. The increase of switching frequency along with the introduction of the important dead time that is required to correct the operation of the inverter, provides a distortion of the output current and voltage waveforms. This affects the ability of the system to reach instability.

In three-phase PWM inverters, the lower and upper switches of each leg alternately turn on and off. The delay of current switching-off for real switches (for example in bipolar transistors), mainly caused by carriers storage time, causes the short conduction time of both switches. This means a short circuit of the dc current source U_d of the dc link. The elimination of this phenomenon may be achieved by introducing dead time t_d into the control system (Figure 4).

In Figure 4, the dead time includes the switching-off time t_{off} of the transistor and the time in which any of the transistors conducts. For analysis of the effect of dead time on the inverter operation, the following assumptions have been considered:

- The switch-off interval time, t_{off}, is neglected.
- Switching frequency is significantly higher than the frequency of the reference voltage.
- The distortion of the output voltage caused by dead time occur at equal interval times.
- During analysis of the output voltage, it is assumed that the output current is nearly sinusoidal.

Therefore, the effect of the repeated switching delay, which provides output voltage distortion, may be described as square waveform with amplitude:

$$\Delta U_{td} = M \cdot t_d \cdot f \cdot U_d, \tag{15}$$

where U_d is the dc bus voltage, M is the number of switchings during an output voltage period, T_d is the delay time, and f is the frequency of output voltage.

In Figure 5, the modulated voltage is shown. In modern motor drives, the control of inverters is realized using the space vector control method. A compensation of the dead-time effect is realized using a microprocessor control system. The inverter output voltage vector during the dead time is described by the direction of output current. On the basis of current vector direction, the time delay shift is described. The compensation rule is shown in Figure 6. This rule depends on checking the output current direction for each phase, when both transistors do not conduct.

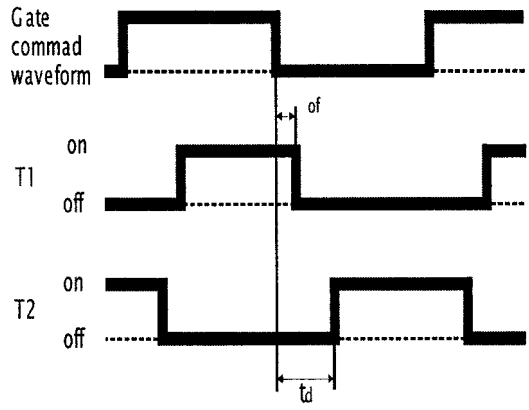

Figure 4. Waveforms of switching control signals for the transistors of one inverter leg with dead time.

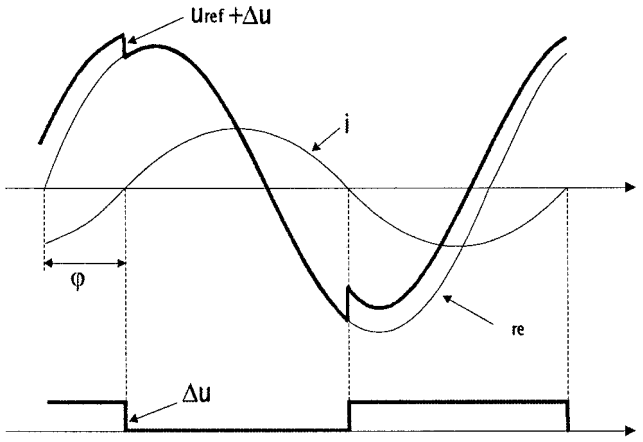

Figure 5. Voltage distortion caused by dead time: U_{ref}, reference sinusoidal output voltage; Δu, distorted voltage in the phase conducting current; i, fundamental current component, and φ, phase angle between current and reference voltage.

The transistor switching time should be properly modified depending on the phase output current direction.

The relation that describes the modified switching time of transistors is of the following form [7]:

$$t_{U,V,W}^{\text{mod}} = t_{U,V,W}^{cal} + t_d \cdot \text{sgn}(i_{U,V,W}), \tag{16}$$

where

$t_{U,V,W}^{\text{mod}}$ modified switching time of transistors
$t_{U,V,W}^{cal}$ calculated switching time of transistors
$i_{U,V,W}$ output phase current.

Accuracy in determining stator current has a significant influence on the calculation of state variables. Current controllers used in a control system should predict current and the PWM block should compensate influence of the dead time, as shown in Figure 7.

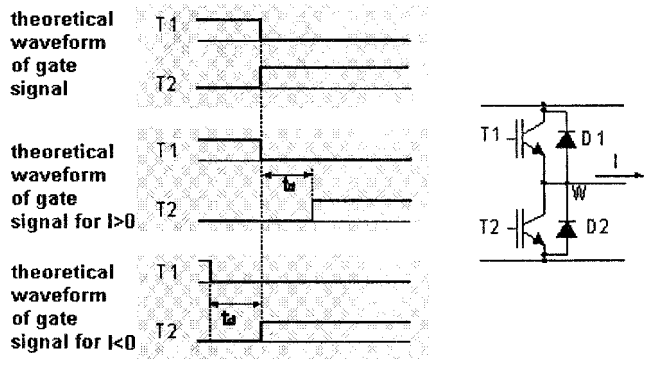

Figure 6. Time delay compensation with space vector PWM.

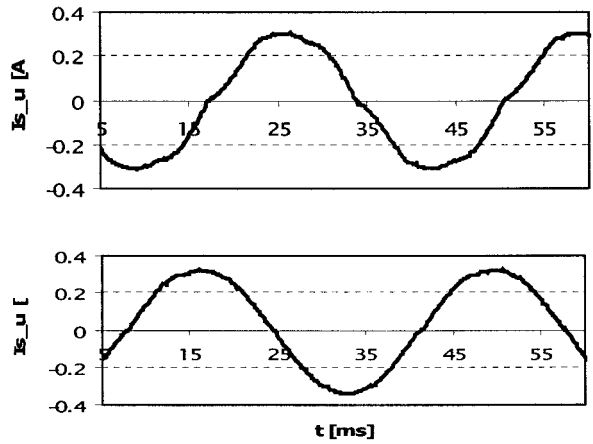

Figure 7. Motor current without and with dead-time compensation.

5. Practical Limitations during Microcomputer Realization of Space Vector PWM

Realization of the previously discussed PWM algorithm is faced with limitations caused by the generation of deadbands. This is due to the specific instant of transistors switching on and switching off and with computer-realization time of the algorithm. The inverter output voltage is generated in the interrupt system. Assuming that interrupts in the microcomputer system require a realization of commands to be sent to the stack for data to be read from the memory and for the realization of logic operations. For these commands, a given time that describes the minimum duration time of the output generated voltage vector should be expected. If the direction of output voltage is similar to the arbitrary active vector, then the calculated time may be less than the minimum time required for the interrupt service routine. Neglecting these times results in an imprecise generation of output voltage vector.

The problem of generating a small interval of time becomes more significant, if the switching frequency is increased, because the ratio between a minimum vector's switching time to the switching period is increased.

6. Modification of PWM Algorithm

Realizing small switching-on time intervals for appropriate vectors (Figure 8), in a traditional implementation of PWM algorithms, is not possible when using microprocessors without already integrated PWM modules or without using additional logic systems. Therefore, our intent is to provide a new PWM algorithm for solving this problem. In practice, two conditions could appear for important implementation of minimum vectors:

1. Output voltage is high and the command voltage vector lies near one of the six active vectors.
2. The inverter output voltage is small.

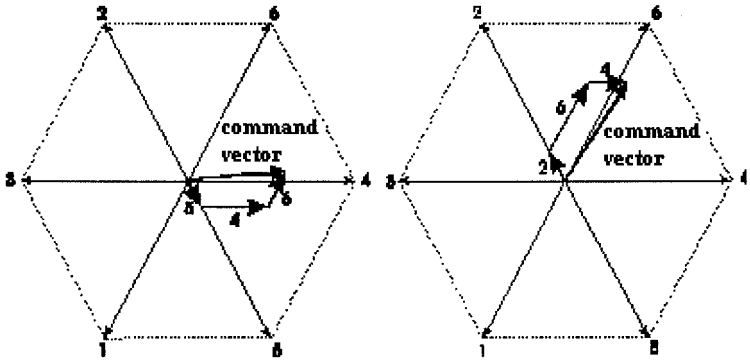

Figure 8. Realization of output voltage vector.

6.1. *Condition 1*

In the first condition, we propose to obtain an output voltage by introducing an additional vector to the vectors combination from the nearest sector. The number of additional vectors depends on the actual position of the reference (commanded) voltage vector. The calculation algorithm for proper switching-on instants of the vectors undergoes some changes in comparison to the previously discussed method. It is suggested that the intervals t_{1v} and t_{2v} (interval times of active vectors while neglecting dead time) are calculated from (12) and (13). The time of switch-on intervals of the third active vector t_m is the minimum switching-on interval time that may be practically realized, and times t_1 and t_2 are modified accordingly. A switching period T_{imp} consists of $T_{imp} = t_0 + t_1 + t_2 + t_m$. Therefore, we can declare the interval times of each switching on time:

$$\begin{aligned}
&\text{When } t_1 > t_m: \qquad t_1 = t_{1v} - t_m; \quad t_2 = t_{2v} + t_m; \quad t_3 = t_m;\\
&\qquad\qquad\qquad\quad t_0 = T_{imp} - t_{1v} - t_{2v} - t_m\\
&\text{When } t_1 < t_m: \qquad t_2 > t_m \quad t_1 = t_{1v} + t_m; \quad t_2 = t_{2v} - t_m; \quad t_3 = t_m;\\
&\qquad\qquad\qquad\quad t_0 = T_{imp} - t_{1v} - t_{2v} - t_m
\end{aligned}$$

Furthermore, to guarantee a minimum number of transistors switching, the proper sequence of vectors switching on should be provided. Therefore, when $t_2 < t_m$ the next sequence to be used should be z_2-n_3-n_1-n_2-z_2-n_2-n_1-n_3, and when $t_1 < t_m$ the next sequence used is z_1-n_1-n_2-n_3-z_1-n_3-n_2-n_1. The selection of a zero vector and the third vector depends on the area in which the actual vector lies and on which time (t_1 or t_2) is less than the time t_m (see Table 2).

6.2. *Condition 2*

In the case of small output voltage, the time t_0 has a large value, close to T_{imp}, but the intervals t_1 and t_2 have values less than T_{imp}. It is possible to realize small output voltage vectors by different combinations of the remaining active vectors. In this work, two methods are suggested for realizing the output vectors: using three active vectors (3AV) and using four active vectors (4AV). In Figure 9, the idea of realizing inverter output voltage vectors is shown.

Table 2
The sequence of switching on vectors with high output voltage

				n_3		
Sector	z_1	n_1	n_2	$t_2 < t_m$	$t_1 < t_m$	z_2
I	0	4	6	5	2	7
II	7	6	2	4	3	0
III	0	2	3	6	1	7
IV	7	3	1	2	5	0
V	0	1	5	3	4	7
VI	7	5	4	1	6	0

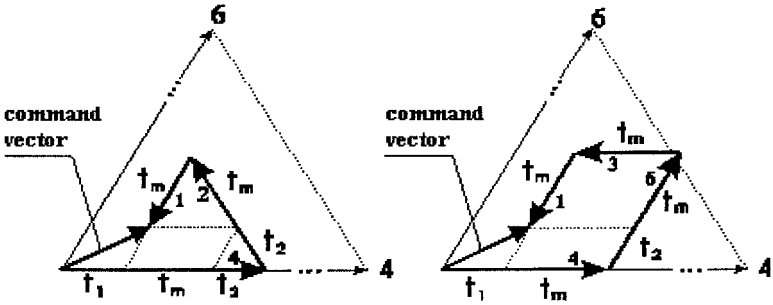

Figure 9. Two methods for realizing the output small vectors.

In this algorithm, a method for calculating the intervals t_{1v}, t_{2v} does not change and depends on (13) and (14). The switching-on instants of each vector are calculated from the following:

$$\text{“3AV”:} \quad t_1 = t_{1v} + t_{2v} + t_m; \quad t_2 = t_{2v} + t_m; \quad t_3 = t_m;$$
$$t_0 = T_{imp} - t_{1v} - 2t_{2v} - 3t_m$$
$$\text{“4AV”:} \quad t_1 = t_{1v} + t_m; \quad t_2 = t_{2v} + t_m; \quad t_3 = t_m; \quad t_4 = t_m;$$
$$t_0 = T_{imp} - t_{1v} - t_{2v} - 4t_m$$

In the “3AV” method, the cycle of vectors switching on, z_1-n_1-n_2-n_3, is used. In this method, it is important to switch over the inverter transistors in two legs simultaneously. In the 4WA method, the next switching-on cycle, n_1-n_2-z_1-n_3-n_4, is used to minimize the inverter losses. Compared with the previous switching cycle, there is only one case in which it is necessary to switch on the inverter transistors in two legs at the same time. The numbers of the suitable vectors are shown in the Table 3.

7. Simulation Investigation of the Exact Voltage Generation Algorithms

The algorithms where realized use C++. Higher harmonic components of the output voltage for different parameters like commanded output voltage, minimum

Table 3
Vectors switching sequences during small output voltage

	Vector								
	4AV method					3AV method			
Sector	z_1	n_1	n_2	n_3	n_4	z_1	n_1	n_2	n_3
I	7	4	6	3	1	0	4	2	1
II	0	6	2	1	5	7	6	3	5
III	7	2	3	5	4	0	2	1	4
IV	0	3	1	4	6	7	3	5	6
V	7	1	5	6	2	0	1	4	2
VI	0	5	4	2	3	7	5	6	3

switching-on time interval, and switching frequency have been analyzed. For a simple comparison between algorithms, all investigations for the same output voltage frequency (50 Hz) and for the same switching frequency (2 kHz) have been utilized. In Figure 10, the waveforms of the inverter output line voltage are shown. In Figure 10, the changes in the output voltage waveform when using the proposed modulation are observed. When the first harmonic passes through zero, additional voltage pulses occur in this area. By observing the harmonics of the output voltage (Figures 11–14) we can observe better waveforms when providing additional vector, when the commanded vector occurs near one of the six active vectors. In the case of traditional PWM algorithm, the command value of the first harmonic has not been reached and the magnitude of the harmonics has increased depending on the switching frequency.

From the results, for small commanded output voltage, it can be assumed that in both cases, the commanded value of the first harmonic is obtained. In the 3AV method, lesser values of the higher harmonics resulted. Since both methods use the same switching frequency, it is better to use the 3AV method. The waveform of line output voltage during the modulation with 3WA method is shown (Figure 15). This also simplifies the control system algorithm in comparison with the 4AV method.

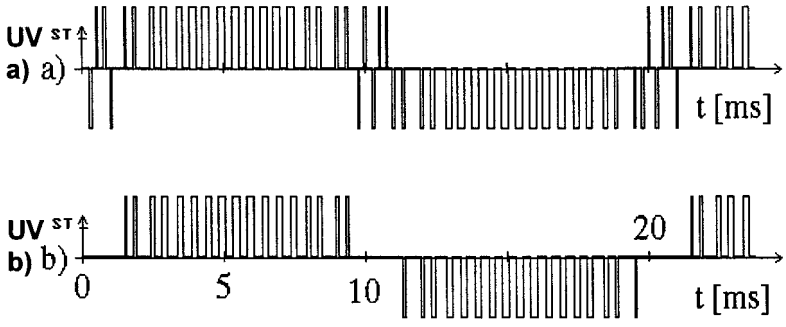

Figure 10. Waveforms of the output line voltage during (a) the proposed modulation and (b) during the traditional PWM method with deadbeat control.

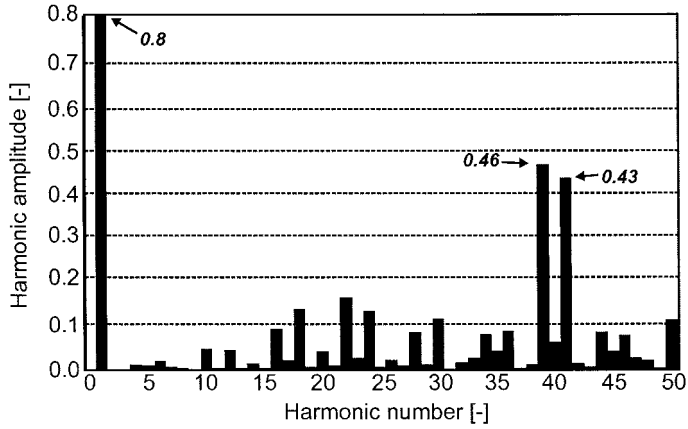

Figure 11. Amplitudes of the harmonics when using the proposed PWM algorithm ($U_{out} = 0.8$ p.u., $U_{1h} = 0.8$ p.u., $t_m = 20$ μs).

A selection of modulation algorithms depends on the requirements desired from the drive control system. The changes are not necessary in simple volts/Hz control systems, but are necessary in the vector control of induction motors because it is essential to get accurately defined values of the output voltage first harmonic.

8. Experimental Verification of the Proposed Algorithm

The presented stator current controller system has been experimentally investigated using a 1.5 kW squirrel cage induction motor and IGBT transistorized voltage inverter. The control system is implemented on a TMS320C50 digital signal processor board. In the control system described, an FPGA system from the FLEX6000 family is also used. The FPGA system makes it possible to realize parts of the control system by hardware that unloads the processor from parts of the realized tasks. FPGA in the discussed experimental setup realizes the following functions: timing

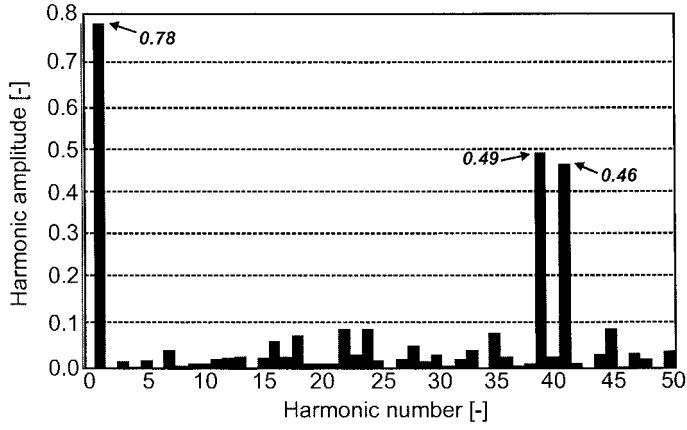

Figure 12. Amplitudes of the harmonics when using the traditional PWM algorithm for $U_{out} = 0.8$ p.u., $U_{1h} = 0.78$ p.u., $t_m = 20$ μs.

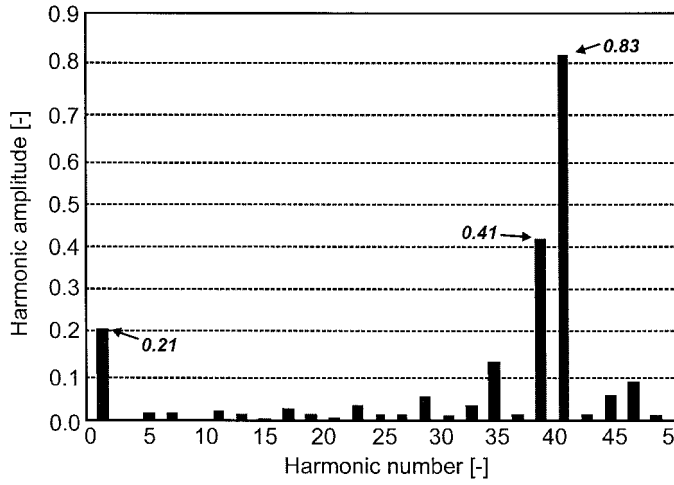

Figure 13. Amplitudes of the harmonics when using 4WA method for $U_{out} = 0.2$ p.u., $U_{1h} = 0.21$ p.u., $t_m = 20$ μs.

of switch-on of each transistor for one switching period, providing a dead time, control of breaking transistor, service of A/D converters, shut-down of inverter in case emergency signals exist, and data transfer between DSP board and the drive system. The experimental results presented are obtained using predictive current controller and closed loop system control with nonlinear control method [7]. On the DSP board, predictive stator current controllers in the open loop system (without the main control system) have been realized. The set values are amplitude and stator current frequency. The performance of the system was investigated by observing the response after a step change of the set value of current magnitude or frequency. The results obtained are presented in Figures 16 to 18, both in the time domain and phase plane. The results obtained show that the proposed algorithm operates correctly.

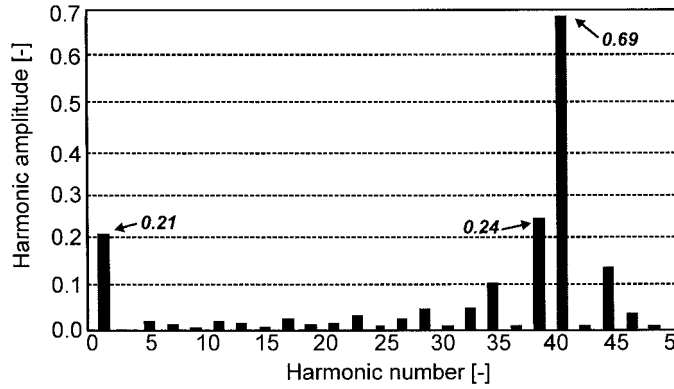

Figure 14. Amplitudes of the harmonics when using 3WA method for $U_{out} = 0.2$ p.u., $U_{1h} = 0.21$ p.u., $t_m = 20$ μs.

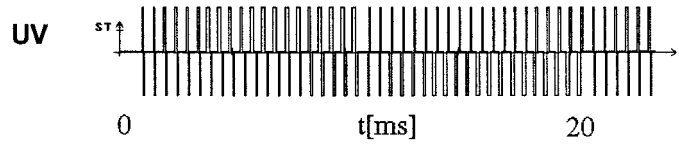

Figure 15. Waveforms of line-output voltage during the modulation with the 3WA method.

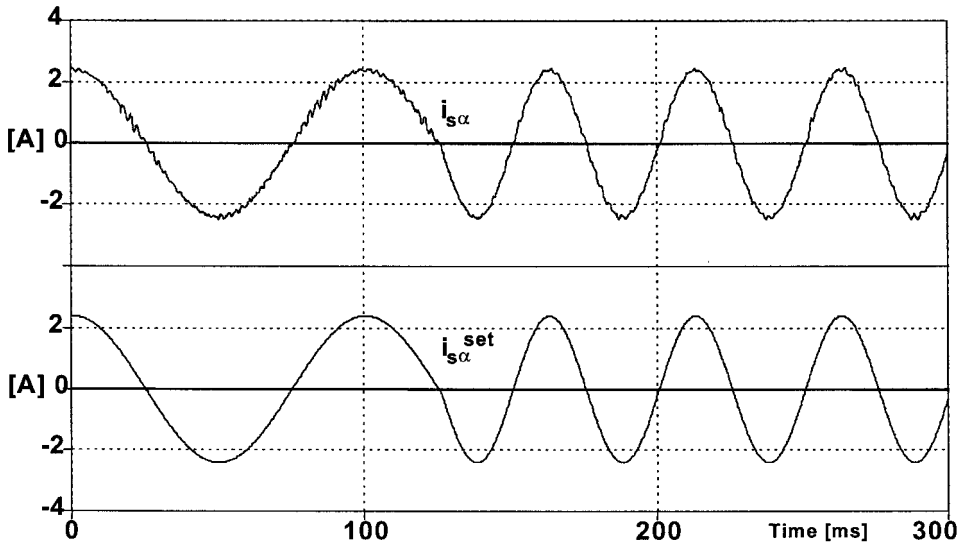

Figure 16. Inverter output current's waveforms. Step change of current frequency set value from $f_i = 10$ Hz to $f_i = 20$ Hz when $I_s = 2.2$ A, $T_{imp} = 150$ μs.

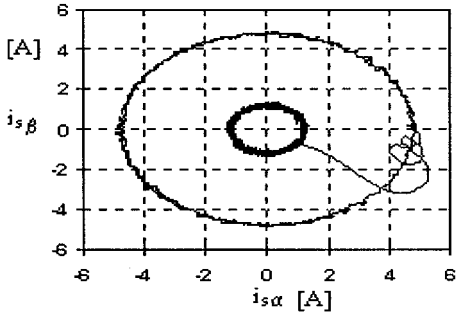

Figure 17. Step increment of current amplitude when $f_i = 10$ Hz and $T_{imp} = 150$ μs.

9. Conclusion

In this article the voltage space vector PWM algorithm for induction motor control is proposed. The problem of exact generation of small voltage vectors is discussed and an appropriate solution is proposed. Two methods for realizing small inverter output voltage vectors are introduced. The influence of dead time is compensated by using the proposed control strategy. The experimental and simulation results show the advantages of the proposed methods. These results are obtained using

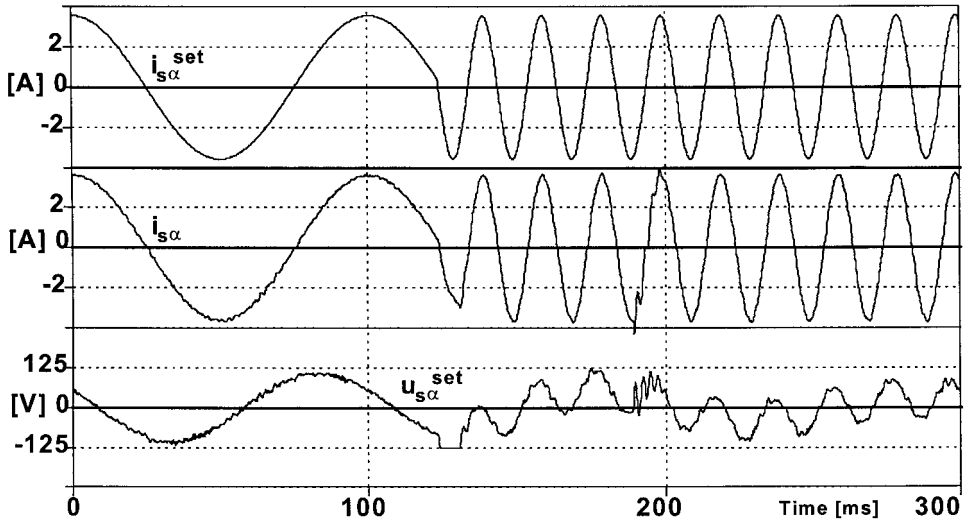

Figure 18. Waveforms of inverter output currents. Step change of current frequency set value from $f_i = 10$ Hz to $f_i = 50$ Hz when $I_s = 2.2$ A, $T_{imp} = 150$ μs.

fixed-point DSP and a programmable system FPGA. Practical realization of the proposed algorithm is discussed.

The use of proposed voltage vector generation methods makes it possible to use the command voltage instead of a measured one in the closed-loop control system. This advantage makes it possible to avoid the delay caused by measurement and conversion process of signals.

Based on the results presented, it is possible to confirm that the developed method works correctly and the desired currents needed by the induction motor are generated.

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