An Earth Fault Current Limiter Using a Modular Multilevel Inverter for Smart Grids Operation

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An Earth Fault Current Limiter Using a Modular Multilevel Inverter for Smart Grids Operation

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***Abstract*—In this paper, a modular multilevel inverter is proposed as an earth fault current limiter. The modular multilevel inverter is designed to limit the earth fault current following a preset current reference. The topology, structure, and functionality of the modular multilevel inverter are introduced. The inverter is designed to be sourced by charging capacitors from the grid itself. The modular multilevel inverter acts as an adjustable impedance to decrease the earth fault current passing in the grid down to safe levels. The control system of the inverter is designed to achieve the desired impedance needed to reduce the earth fault current to predetermined values, which do not cause any damage to the grid or its protection components, but sufficient to activate the protection system. Besides, the modular multilevel inverter does not need very high voltage rating devices, as the maximum voltage rating of each switch does not exceed 650 V. Such a modular multilevel inverter has a low Total Harmonic Distortion in the grid's voltages, even with low values of the passive components of the coupling filter. Moreover, with the proposed system, the grid can continue supplying the load with the needed power even during the ground fault. Simulations are carried out using MatLab/Simulink platform and various results demonstrate the ability of the proposed system in controlling the ground fault current.**

Keywords—ground fault, multilevel inverter, proportional resonant controller.

I. INTRODUCTION

The earthing system requires one point to be connected to ground, either solidly or through impedance to create a path for the fault current. The high fault current occurring due to different kinds of faults reduces the life-time of the network equipment rapidly and increases maintenance cost. In order to increase safety and to diminish the damages in the network, the earth fault current has to be reduced. Limiting the fault current using the power electronic converters creates a new reliable, efficient and inexpensive method with low Total Harmonic Distortion (THD), increasing the life time of circuit breakers and other system components in general.

Fault current is the main reason of decreasing the life-time of the grids requiring high maintenance cost making the service unreliable and inefficient. The fault current issue is a common problem occurring in transmission lines and distribution systems. It results from many environmental reasons or human mistakes [1]. In general, there are two main types of faults; symmetrical faults such as three phase to ground fault, and asymmetrical faults such as phase to ground faults, phase to phase faults, and phase to phase to ground faults. Single line to ground fault is the most frequent fault occurring amongst other types of faults [2].

The system grounding is the connection between the transformer neutral point and the earth. Safe grounding design has two objectives: the first one is the ability of carrying the currents into earth under normal and fault conditions without exceeding the grid's and the equipment limits. The second is protecting people from the danger of electric shock and achieve the highest safety for them [3]. The diagram in Fig. 1 summarizes the types of grounding techniques. These techniques are: solid grounding, resistance grounding, reluctance grounding, and the power electronic grounding by connecting the neutral of the system via a power electronic converter, which limits the ground fault current to a predetermined value set via a controller [4]–[6]. The latter technique introduces a new scope in the design of the protection system, increasing the reliability and reducing the cost of the grid. Moreover, the power electronic converter provides variable impedance that could be used also for other functions during normal operation. The various types of power electronic converters expand the ability of appropriate selection.

Pulse Width Modulation (PWM) techniques are used to generate the gate signals of the switches in a power electronic converter. For multilevel inverters, multicarrier PWM techniques are used. The multicarrier PWM techniques are based on a single modulating or reference signal, which in

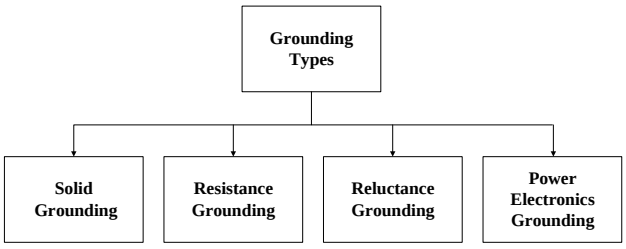

Fig. 1. Classification of neutral grounding techniques

most cases has a sinusoidal form. This reference waveform is compared with a number of triangular waveforms, using a PWM technique, which has many benefits such as; reduction of low frequency harmonics, reduced THD, and easy to implement and control, but it also attenuates the fundamental components [7]. PWM techniques are classified as:

- Carrier disposition methods, such as: Phase Disposition (PD), Phase Opposition-Disposition (POD), Alternate Phase Opposition-Disposition (APOD) [8]
- Sub-harmonic methods: Saw-tooth and Triangular

In a Carrier disposition method, N-1 triangular signals, with the same frequency and same peak-to-peak amplitude, are disposed such that the bands they occupy are continuous and form an N-level output waveform. In the PD method, all triangular carriers are in phase. The significant harmonics are present at sidebands of the carrier frequency. In a Sub-harmonic method, a number of carriers are phase shifted from each other, where the phase-shift angle is determined by the number of levels in the output waveform. This is defined as θ = 360º/N-1, where N is the number of line-to-neutral levels. Saw-tooth signals have the same amplitude, but they are out of phase [9].

II. Multilevel Inverters

A. Cascaded H-Bridge Inverter

A Cascaded H-bridge inverter consists of multiple single-phase H-bridge inverters, with their outputs connected in series. The number of cells determines the output level. With higher levels, the output voltage wave becomes closer to sinusoidal with very low harmonic content. The switching power losses are very low per cycle, which increases the reliability of the inverter. Besides, the cost is reduced due to less employed semiconductors. Each cell is provided by a separate dc source, which might be considered as a drawback. A high switching frequency PWM technique is required [10].

B. Diode-Clamped Multilevel Inverters

Diode-Clamped multilevel inverters share the same dc source for each phase of the three phases, which decreases dc cabling and losses on the dc side. Diodes are used to clamp the dc bus voltage, in order to achieve multilevels in the output voltage [11]. Thus, this inverter uses diodes to limit the power electronic devices' voltage stress. By increasing the number of voltage levels, the quality of the output voltage is improved and filters, needed to reduce harmonics, can be eliminated, but a greater number of diodes are required [12]. When operating at high voltage levels, the diodes are subject to different voltage stresses.

C. Double Star Multilevel Inverter

The modules of the Double Star Inverter are aligned in one leg only [13]. Moreover, the output voltage is the voltage between the positive terminal of the upper module and the negative terminal of the lower module. Besides, the output of each leg of the inverter always has a dc component. The output voltage (V_{out}) has dc and ac components, and is given by "(1)":

$$V_{out} = V_{DC} + V_{AC} \quad (1)$$

The output peak voltage ($\hat{V}_{out}$) is represented by:

$$\hat{V}_{out} = \frac{M*N_i*V_{mod}}{2} \quad (2)$$

where M is the Modulation index, N_i is the number of modules in the inverter leg, and V_{mod} is the dc voltage of each module.

Increasing the modules in the Double Star Inverter leads to decreasing the Total Harmonic Distortion (THD). On the other hand, increasing the number of modules increases the cost, the complexity and the losses within the inverter. This type of inverters, has one modulating and a group of triangular signals. The triangular signals are compared with the modulating signal such that; the output of the comparison per each triangular signal yields '1' whenever the modulating signal is higher than the triangular signal, and is '0' otherwise.

D. Modular Multilevel Inverter

The topology of a Modular Multilevel Inverter is shown Fig. 2. Each module is built as shown in Fig. 3. The modules in this topology are arranged in two symmetrical legs. Each leg consists of cascaded modules. However, the two legs are connected by their last modules' negative terminals. As the switches in each module are complement to each other, the output of each module may equal the source (capacitor) voltage or zero volt. As a result of symmetry between the legs, the output of this inverter does not have a dc component. Furthermore, the peak of the output voltage ($\hat{V}_{out}$) is proportional to the Modulation index (M) by:

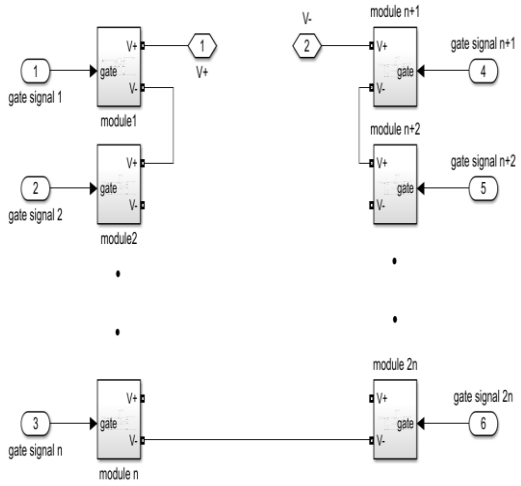

Fig. 2. A modular multilevel inverter topology

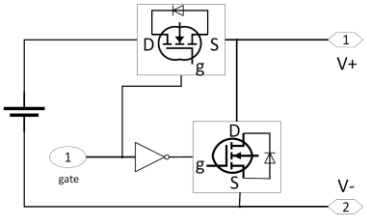

Fig. 3. Module's structure in a modular multilevel inverter

$$\hat{V}_{out} = M * N_m * V_{DC} \quad (3)$$

such that,

$$M = \frac{\hat{V}_m}{\hat{V}_c} \quad (4)$$

where N_m is the number of modules per leg, $\hat{V}_m$ is the peak of the modulating signal, and $\hat{V}_c$ is the peak of the carrier signal.

The output of the inverter has lower THD, as the number of the modules is increased. On the other hand, increasing the number of modules increases the cost, the complexity and the losses within the inverter. The carrier signals are compared with the modulating signal such that; for the positive carriers, the output of the comparison per each carrier signal yields "1" whenever the modulating signal is higher than the carrier signal. In contrast, the output of the comparison per each negative carrier signal yields "0" whenever the modulating signal is lower than the carrier signal.

III. Modelling and Control of the Proposed System

Fig. 4 shows a flow chart of the proposed fault current limiting technique. The system works when a sudden change is detected in one of the phase voltages. Then a reference current is set and sent to a Proportional Resonant (PR) controller to be compared with the inverter's current, which is approximately the fault current, and so the PR starts operating. Moreover, a signal is sent to the main circuit breaker in order to trip the faulty part of the grid. Although the circuit breaker will trip after three cycles of operation, the control system keeps an eye on the faulty phase voltage; if another sudden change in the same phase voltage is detected before the three cycles elapse, another signal will be sent to the circuit breaker in order to abort the tripping action, and a signal is sent to the PR in order to halt working. Consequently, the inverter will appear as a short circuit (as in normal operation) since the modulating signal is adjusted to be 0 V.

The proposed system has been modelled in order to test the Ground Fault Current Limiting inverter, as shown in Fig. 5. A main generator of 33 kV and 50 Hz is used to feed the grid, and a main D-Y transformer is used to step the voltage down to 11 kV. Moreover, three static symmetric loads are connected radially using a D-Y step down transformer for each load. The loads' rms voltage is 400 V. Furthermore, π-model transmission lines are used to connect between the main transformer and each distribution transformer.

A. Proportional-Resonant Controller

The Proportional-Resonant controller (PR) provides a gain at a particular frequency (resonant frequency) and hence can achieve zero steady-state error and almost no gain exists at the other frequencies [14]. An ideal PR controller may cause stability problems because of its infinite gain at resonant frequency. When the grid has a small frequency variation, the PR controller does not perform properly and the output signal cannot track its reference signal, thus it is difficult to implement. In this case, it is preferred to use a non-ideal PR controller, which has a finite gain that is still high

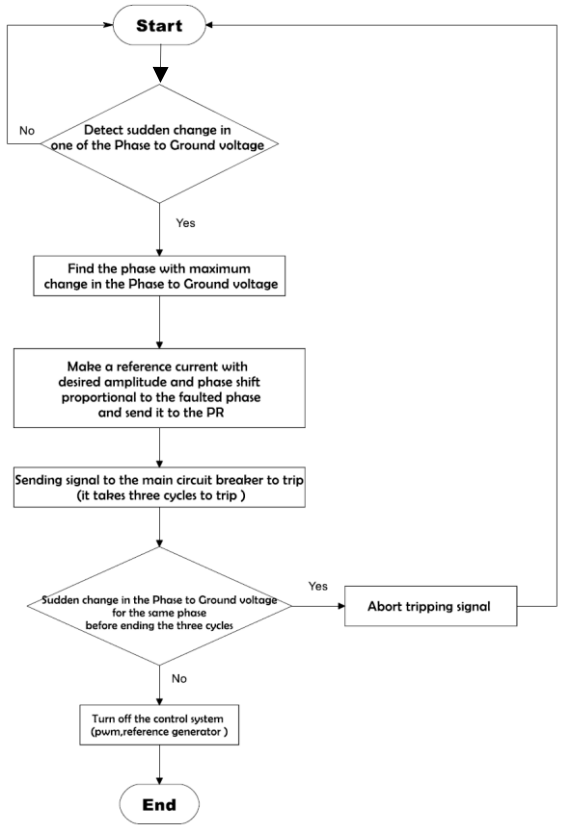

Fig. 4. A flow chart for the fault current limitting technique

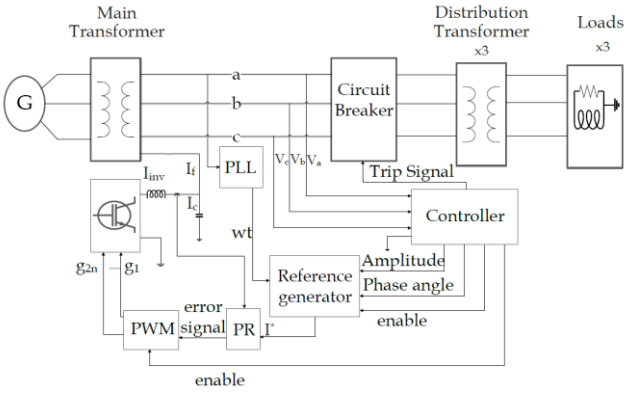

Fig. 5. A block diagram of the simulation system implementing a earth fault current limiting modular multilevel inverter

enough for good tracking to ensure a zero steady state error. The PR transfer function is given by [14]:

$$G_{PR} = K_P * G_{Re} \quad (5)$$

such that,

$$G_{Re} = \frac{K_i * s}{s^{2+}\omega_o^2} \quad (6)$$

where K_P and K_i are gain constants and ω_o is the operating angular frequency.

B. Design of System Components

1. Number of Required Modules

The minimum voltage of the source (capacitor) per module depends on the peak value of the fundamental voltage (V_p), which equals the dc level; i.e.,

$$V_{DC} = V_p = \frac{11K}{\sqrt{3}} * \sqrt{2} = 8981.5\ V \tag{7}$$

Assuming that, each module has a source of 620V, then the number of modules (N_m) is:

$$N_m = \frac{8981.5}{620} = 14.48 \tag{8}$$

Thus, the number of capacitors in each leg is, therefore, 15, the dc voltage is 9kV, and the total number of capacitors (sources) required = 2*15 = 30.

2. LC Filter

Fig. 6 shows the equivalent circuit for the inverter and the LC filter. The capacitor C is the equivalent capacitance of the operating modules in the inverter. Thus, the capacitance value of C is variable depending on the number of the operating modules in the inverter. C_f and L_f are the capacitance and the inductance of the LC filter, respectively. In order to calculate the cut-off frequency of the circuit ($L_f C_f$ filter and C), the transfer function of the simplified circuit, shown in Fig. 6, whose output is the voltage is around C_f, has to be found as:

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{sC_f}}{\frac{1}{sC_f} + \frac{1}{sC} + sL_f} \tag{9}$$

Rewriting the transfer function yields:

$$T(s) = \frac{1}{1 + \frac{C_f}{C} + s^2 L_f C_f} \tag{10}$$

In order to find the cut-off frequency (ω_{cut}), the denominator in "(10)" is set to zero and the 's' is transferred to 'jω', yielding:

$$\omega_{cut} = \sqrt{\frac{C_f + C}{L_f C_f C}} \tag{11}$$

Fig. 7 shows the inverter, the $L_f C_f$ filter and Thevenin's circuit seen by the filter and the inverter during a ground fault. Applying KCL to the filter's capacitor node in Fig. 7 yields:

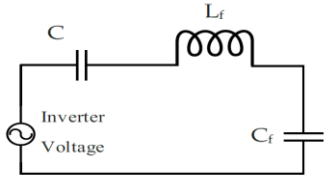

Fig. 6. The equivalent circuit for the inverter and the LC filter

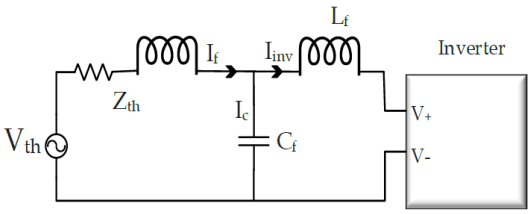

Fig. 7. Simplified circuit of the system during a ground fault

$$I_f = I_c + I_{inv} \tag{12}$$

where I_f is the fault current, I_c is the current passing through the capacitor and I_{inv} is the inverter's current. In order to have an accurate current control, I_{inv} must be almost the same as I_f. Thus, I_c should be minimized, such that:

$$|I_C| = \frac{|V_c|}{|Z_{C_f}|} \tag{13}$$

If the filter capacitor's maximum voltage equals the phase voltage, and the current passing through the capacitor is 1 A, then:

$$V_C = \frac{11K}{\sqrt{3}} = \frac{1}{\omega C_f} \tag{14}$$

$$C_f = \frac{\sqrt{3}}{2\pi(50)\ (11K)} = 5 * 10^{-7}\ F \tag{15}$$

3. Module's Capacitor (C_m)

The voltage ripple at each capacitor (ΔV) is:

$$\Delta V = \frac{1}{C_m} \int_a^b i(t)dt \tag{16}$$

where $'a'$ and $'b'$ are the time boundaries of a charging or discharging period. Further rearrangement of "(16)" and assuming $i(t) = Isin(\omega t)$ result in an expression for the capacitor (C_m) value as:

$$C_m = \frac{I\ (\cos(\omega a) - \cos(\omega b))}{\omega * \Delta V} \tag{17}$$

For the worst scenario of a charging and discharging period, $\cos(\omega a) = -\cos(\omega b)$, therefore:

$$C_m = \frac{2I\ (\cos(\omega a))}{\omega * \Delta V} \tag{18}$$

Assuming the maximum peak fault current is set to 600 A, and ΔV is 3 V, during the first cycle of the fault current, yields:

$$C_m = \frac{2(600)\ (\cos(\omega a))}{(2 * \pi * 50) * 3} = \frac{4\cos(\omega a)}{\pi} \tag{19}$$

If the capacitors in the modules have the same value, then $C_m = 1.274\ F$. The minimum value of the equivalent capacitance of the modules 'C' occurs when the whole modules in the inverter are on. Hence, $C = \frac{C_m}{15} = 0.0849\ F$. Recalling "(11)", C_f in the numerator can be neglected yielding the cut-off angular frequency as:

$$\omega_{cut} = \sqrt{\frac{C}{L_f C_f C}} \quad (20)$$

Therefore,

$$\omega_{cut} = \frac{1}{\sqrt{L_f C_f}} \quad (21)$$

The cut-off frequency is selected such that:

$$10\omega_o < \omega_{cut} < \frac{1}{2}\omega_s$$

$$10f_o < f_{cut} < \frac{1}{2}f_s$$

For $f_s = 10\,kHz$ and $f_o = 50\,Hz$, choosing $f_{cut} = 4\,kHz$, and using $C_f = 5 * 10^{-7}\,F$, as obtained from (15)", "(21)" yields:

$$L_f = \frac{1}{C_f * \omega_{cut}^2} = 3.17\,mH \quad (22)$$

IV. Simulation Results

The simulation model of Fig. 5 was used to emulate two types of faults; the first fault was conducted to demonstrate the effect of the reference current angle on the state of charge of the capacitors of the modules. Another fault was conducted to demonstrate the effectiveness of the proposed system in controlling the ground fault current. For the first fault, the fault was imitated to occur in phase "a" at the secondary of the main transformer at t = 0.02 s, and lasts for three cycles. The voltage of the phases with respect to ground are shown in Fig. 8. It is clear that, the healthy phases' voltages (V_b and V_c) increase with respect to ground when the fault occurs. Their voltages' values become closer to each other when the fault current decreases. The angle of the reference current, which is the phase shift between the reference current and phase "a", was set to π during the first cycle of the fault. In the second cycle, the reference angle was set to $\frac{\pi}{2}$, whilst it was set to 0 in the last cycle. The voltages of all capacitors in the left leg (the leg which is responsible for providing the voltage in the negative half cycle) were monitored, as shown in Fig. 9. The capacitors were charging in the first cycle. In the second cycle, the capacitors have started to discharge for a quarter of the cycle, then they started charging again. Thus, during the second cycle, the overall change in charge state is almost 0.

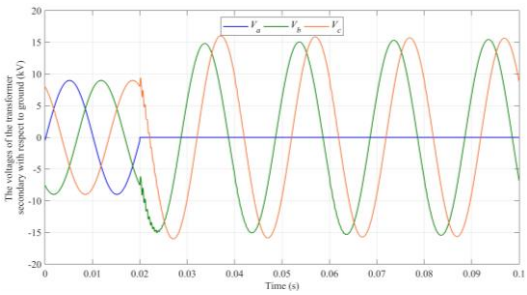

Fig. 8. The voltages of the transformer secondary with respect to ground

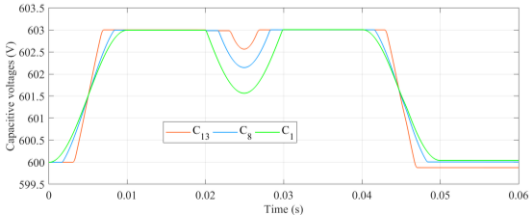

Fig. 9. The voltages of the low, middle, and high modules' capacitances in the left leg of the inverter

The second fault occurred under similar conditions to those of the first one, with the current reference angle set to π, to demonstrate the effectiveness of the system in controlling the ground fault current. The PR controller's reference current peak value was set to 600 A, and then reduced by 200 A /cycle of the fault period, for three cycles. The PR controller forced the inverter's current, which approximates the fault current, to track exactly the reference current, as shown in Fig. 10 a). Although, there is a small difference between the fault current and the inverter' current, absorbed by the capacitor, the inverter's current and the fault current are almost identical apart from the instant of initiating the fault at t = 0.02 s, as can be seen from the waveforms of Fig. 10 b). The filter's capacitor current is shown in Fig. 11.

The faulty phase will see the inverter as a load, so the current in the inverter and the capacitor of the LC filter are part of the faulty phase current, besides the load's current. Fig. 12 shows an increment in the current of phase "a", which increased from 800 A during normal operation to 1400 A during the first cycle of the fault. This increment is the current drawn by the capacitor and the inverter. Moreover, the currents are decreasing each cycle post the fault occurrence, as the reference current is decreased in steps (200 A/cycle). This fault current can be compared with the solid ground fault current shown in Fig. 13, which was obtained when a solid neutral to ground link replaced the proposed modular multilevel inverter. It is clear that, the current levels are very high, reaching a peak value of about 5,000 A.

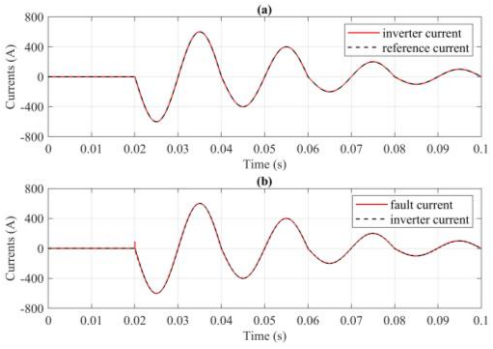

Fig. 10. a) The inverter's current and the reference current, b) the inverter's current and the fault current are almost identical.

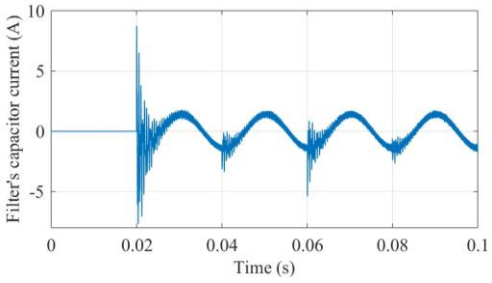

Fig. 11. The filter's capacitor current

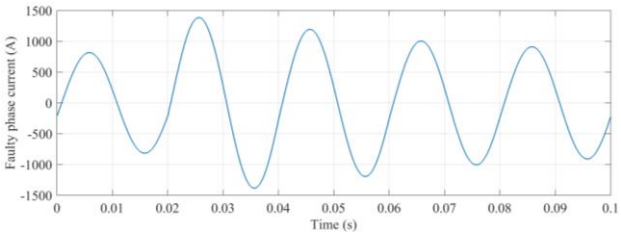

Fig. 12. Faulty phase current prior and post fault

Fig. 14 shows that, the voltages of the main transformer were affected only at the beginning of the fault, then they are back to normal values. Hence, the loads continued to work normally during the fault. The load voltages are not affected as much as the main transformer's voltages, because each load has its own distribution transformer, which in turn works as a low pass filter (because of the inductance of the windings). When the voltages in Fig. 14 were analyzed using the FFT algorithm in MatLab/Simulink, the results showed extremely low THD (less than 1%), which can be anticipated from the cleanliness of the waveforms in Fig. 14. Fig. 15 shows the inverter's unfiltered and filtered voltages, overlapping each other, prior and during the fault. The latter figure demonstrates the ability of the modular multilevel inverter and the PR controller in producing a voltage equal to that of the faulty phase, phase 'a', but in opposite polarity, which results in the load voltages being not affected by the fault, as was seen in Fig. 14; the grid continues feeding the loads during the fault normally until the circuit breaker trips.

V. Conclusions

The proposed system introduces a modular multilevel inverter operating as a ground fault current limiter. This topology detects the sudden change in the phase-ground voltage, and determines the faulty phase. Moreover, the controller sets a reference current, with the desired amplitude and phase shift, which controls the ground fault current and forces it to track the preset signal. Thus, protecting all components of the grid from the harmful high fault currents. A tripping signal is sent to the main circuit breaker to activate the tripping action in the appropriate time. Moreover, the capacitors' voltages are controlled to be charged or discharged at will.

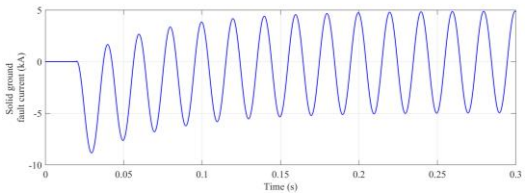

Fig. 13. Solid ground fault current without a current limiter

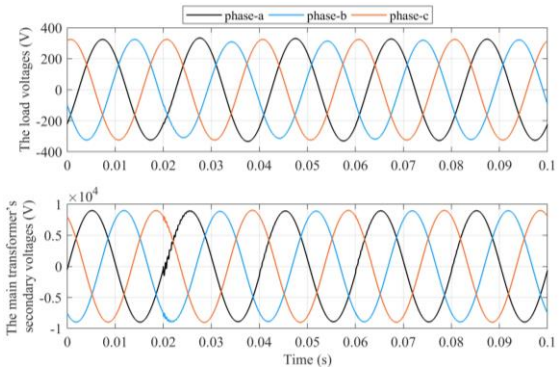

Fig. 14. The load voltages and the main transformer's secondary voltages, from top to bottom, respectively

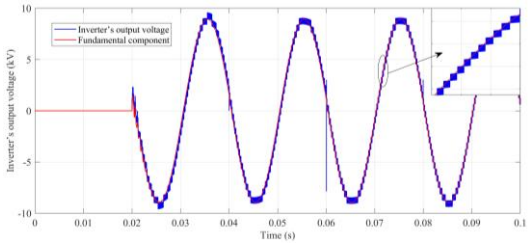

Fig. 15. Unfiltered and filtered inverter's output voltage (neutral-ground voltage) during a fault, overlapping each other

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