Control of Solid-State Fault Current Limiter for DG-Integrated Distribution Systems

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***Abstract*—Fault current limiter (FCL) is a device that limits the system current under fault conditions without disconnecting the system and affecting the power system protection components such as circuit breakers. Many types of FCLs have been proposed to limit the magnitude of the fault current. Solid-state fault current limiters (SSFCLs) can limit the peak value of the fault current by applying several methods, such as controlling the system impedance or controlling the voltage that appears across the fault. In this paper, a new control scheme for the SSFCL circuit is presented. The control method is based on controlling the duty cycle of solid state switches to control the rms value of the system fault current. Numerical simulations using Matlab/Simulink confirm the technical features of the presented control method of SSFCL.**

Keywords— fault current limiter; solid state fault current limiter; distributed generation; duty cycle

I. INTRODUCTION

In smart grids, renewable energy based distributed generation (DG) units are integrated with the system distribution level [1]. Power electronic converters are used to increase the grid power quality and integrate DG units into electric power systems. However, the DG units have an effect on the power system protection requirements since it has been designed to protect the system without considering the integration of DG units [1]-[3].

Dealing with fault currents in power systems is very important in order to avoid a physical damage to the DG unit, to provide high availability of the system and to increase the power quality of the system. The fault currents become larger when the DG units are integrated with the distribution level. [5]. As a result, the circuit breakers will not be able to clear these fault currents if the peak value of fault current is uncontrolled. This high fault current can lead to mechanical and thermal breakdowns, which leads to oversizing and increased cost [6], [7].

There are many methods that can be applied to mitigate the effect of DG on the power system protection, which can be divided into four schemes: modifying the protection system, using an adaptive protection system, limiting the DG capacity, and using fault current limiters (FCLs). However, these solutions have some disadvantages. Modifying the protection system is expensive and makes the protection system more complex. Adaptive protection requires new systems to be added to the power system protection such as communication infrastructures and fast processing units. Limiting the DG capacity limits its penetration level [4]. So it is a valuable and an interesting topic to compare between FCL strategies and technologies and to propose the best technology to solve protection-related problems without restricting DG utilization during normal conditions.

An advanced current limiting technology, based on using high power solid-state fault current limiters (SSFCLs), is a good solution to the distribution system problems caused by a high fault current in the case when they are integrated with DGs. SSFCLs can limit the fault currents. Therefore, they reduce switching surges, and improve the power quality of the grid [8]-[11].

This paper presents a new control algorithm of SSFCL based on controlling the duty cycle of solid state power switches in order to softly control the peak value of the fundamental component of the fault current. The paper is organized as follows; section II introduces the operating principle of the SSFCL with the proposed controlling scheme, section III provides the simulation results and analyzes all results, and section VI summarizes the main conclusions.

II. STRUCTURE AND OPERATING PRINICPLE OF SSFCL

The structure of the SSFCL is shown in Fig. 1. It consists of a bidirectional switch comprising two IGBTs connected in anti-parallel, S_1 and S_2, to provide a bidirectional current path. Each IGBT is connected in series with a diode to attain reverse blocking capability. A varistor is connected in parallel with the switching devices to protect against excessive transient voltages. It shunts the current created by the excessive voltage away from both switches when they are turned on or off [11]. IGBTs or IGCTs with reverse blocking capability, if available at the required power rating, may be used instead of the non-reverse blocking IGBTs and diodes. Devices with the reverse blocking capability will reduce the power loss in the solid state bidirectional switch, and hence will increase the efficiency.

The operation principle of the bidirectional switch can be explained with reference to the same figure. Under normal conditions, both switches are turned on, and therefore the output voltage is equal to the supply voltage. In this case, the SSFCL acts as buffer circuit and has no effect on the current drawn by the load.

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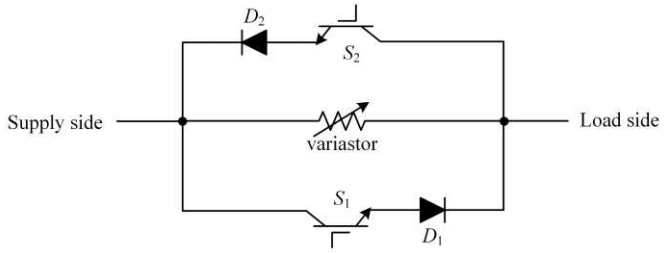

Fig. 1. The stucture of SSFCL circuit.

Under fault conditions, both switches are turned on and off together in order to limit the fault current. S_1 is switched during the positive half cycle, whilst switch S_2 is switched during the next half cycle. Fig. 2 shows the waveform of the limited fault current, i_F.

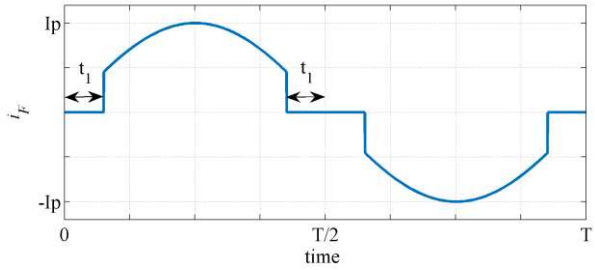

Fig. 2. The instantaneous limited fault current.

An expression of the fundamental component of fault current, $i_{F,1}$, can be derived using Fourier series expansion as:

$$i_{F,1} = a_1 \cos(\omega t) + b_1 \sin(\omega t) \tag{1}$$

where a_1 and b_1 are the coefficients of the Fourier series. The coefficients can be calculated as:

$$\begin{aligned} a_1 &= \frac{2}{T}\int_0^T i_F \cos(\omega t)dt; \\ b_1 &= \frac{2}{T}\int_0^T i_F \sin(\omega t)dt. \end{aligned} \tag{2}$$

Assuming that the fault current is symmetrical in both half cycles and is an odd function, then the value of a_1 equals zero. In this case, $i_{F,1}$ is given by:

$$i_{F,1} = b_1 \sin(\omega t) = I_{F,1} \sin(\omega t), \tag{3}$$

and the coefficient $I_{F,1}$ can be calculated as:

$$\begin{aligned} I_{F,1} &= \frac{2I_p}{T}\left[\int_{t_1}^{T/2-t_1} (\sin(\omega t))^2 dt + \int_{T/2+t_1}^{T-t_1} (\sin(\omega t))^2 dt\right] \\ &= \frac{4I_p}{T}\left[\int_{t_1}^{T/2-t_1} (\sin(\omega t))^2 dt\right] = \frac{2I_p}{T}\left[\int_{t_1}^{T/2-t_1} (1+\cos(2\omega t))dt\right] \\ &= \frac{2I_p}{T}\left[\frac{T}{2} - 2t_1 + \frac{1}{2\omega}\left[\sin(\omega T - 2\omega t_1) - \sin(2\omega t_1)\right]\right] \\ &= \frac{2I_p}{T}\left[\frac{T}{2} - 2t_1 - \frac{1}{2\omega}\left[\sin(2\omega t_1) + \sin(2\omega t_1)\right]\right] \\ &= \frac{2I_p}{T}\left[\frac{T}{2} - 2t_1 - \frac{\sin(2\omega t_1)}{\omega}\right] = I_p\left[1 - \frac{2\omega t_1}{\pi} - \frac{\sin(2\omega t_1)}{\pi}\right] \end{aligned} \tag{4}$$

As a result, the rms value of the fundamental component of the fault current is given by:

$$I_{F,1} = \frac{I_p}{\sqrt{2}}\left[\delta - \frac{\sin(\pi\delta)}{\pi}\right]; \quad \delta = \frac{(T/2 - 2t_1)}{T/2}, \tag{5}$$

where δ is the duty cycle of each switch with respect to half cycle. The rms value of the limited fault current, I_F, can be calculated as:

$$\begin{aligned} I_F &= \sqrt{\frac{1}{T}\left[\int_0^T (i_F)^2 dt\right]} \\ &= \sqrt{\frac{1}{T}\left[\int_{t_1}^{T/2-t_1} (I_p \sin(\omega t))^2 dt + \int_{T/2+t_1}^{T-t_1} (I_p \sin(\omega t))^2 dt\right]} \\ &= I_p\sqrt{\frac{2}{T}\left[\int_{t_1}^{T/2-t_1} (\sin(\omega t))^2 dt\right]} = I_p\sqrt{\frac{1}{T}\left[\int_{t_1}^{T/2-t_1} (1+\cos(2\omega t))dt\right]} \\ &= I_p\sqrt{\frac{1}{T}\left[\frac{T}{2} - 2t_1 + \frac{1}{2\omega}\left[\sin(\omega T - 2\omega t_1) - \sin(2\omega t_1)\right]\right]} \\ &= I_p\sqrt{\frac{1}{T}\left[\frac{T}{2} - 2t_1 - \frac{1}{2\omega}\left[\sin(2\omega t_1) + \sin(2\omega t_1)\right]\right]} \\ &= I_p\sqrt{\frac{1}{T}\left[\frac{T}{2} - 2t_1 - \frac{\sin(2\omega t_1)}{\omega}\right]} \\ &= I_p\sqrt{\frac{1}{2}\left[1 - \frac{2\omega t_1}{\pi} - \frac{\sin(2\omega t_1)}{\pi}\right]} = \frac{I_p}{\sqrt{2}}\sqrt{\left[\delta - \frac{\sin(\pi\delta)}{\pi}\right]} \end{aligned} \tag{6}$$

The total harmonic distortion, THD, of the limited fault current is therefore expressed as:

$$THD = \sqrt{\left(\frac{I_F}{I_{F,1}}\right)^2 - 1} = \sqrt{\frac{1-\delta+\frac{\sin(\pi\delta)}{\pi}}{\delta-\frac{\sin(\pi\delta)}{\pi}}}. \quad (7)$$

According to (5), Fig.3 shows the typical characteristics the normalized fundamental component of the fault current versus the duty cycle of switches for different values of fault resistance, assuming the rated load current is 50 A and it is supplied by a 220 V, 50 Hz AC source. Fig. 4 shows the effect of both fault resistance and duty cycle on the peak value of the fundamental component of the fault current in a 3-D plot. The decrease in the duty cycle and/or the increase in the fault resistance leads to a decrease in the rms value of the fundamental component of fault current.

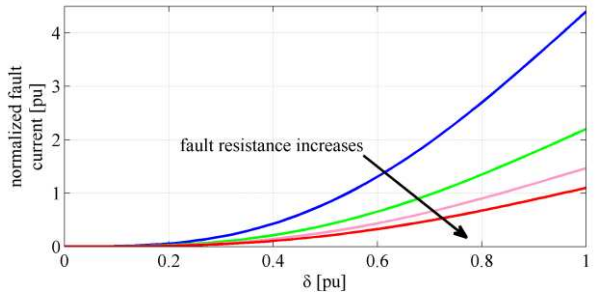

Fig. 3. The magnitude of fault current versus duty cycle of switches in the SSFCL.

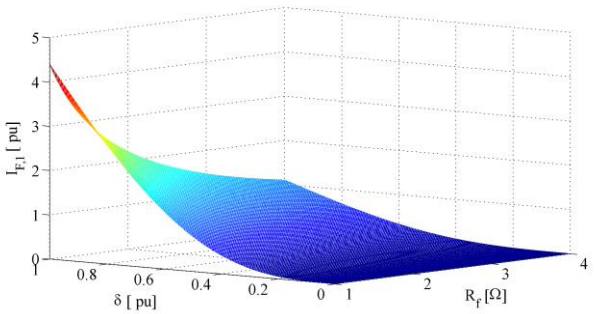

Fig. 4. The 3-D plot of duty cycle, fault resiatnce, and the limited fault current in pu.

Fig. 5 shows the effect of the duty cycle variations on the THD of the limited fault current. It is clear that the THD is independent of the fault resistance as given in equation (7). The THD decreases when the duty cycle of switches increases. Typically, the protection system is set to operate with an rms value of the fundamental component of the fault current which is 2 to 3 times its rated value, and therefore the minimum range of duty cycle operation of the SSFCL is 0.71-0.84. In this case, the THD of the fault current will be in the range of 1.18%-0.46%, which is small enough to avoid derating of protection components.

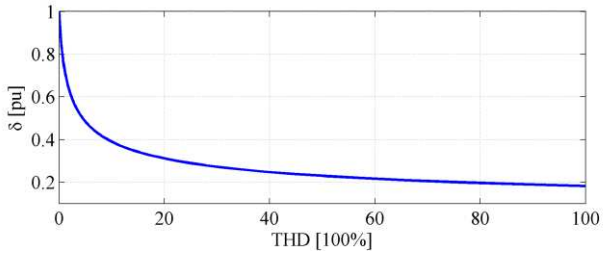

Fig. 5. The duty cycle versus THD.

III. Simulation Results

The operating characteristics of the SSFCL have been tested by means of numerical simulations. In this simulation, an equivalent single-phase SSFCL was simulated to demonstrate the performance of a faulty distribution generation circuit when SSFCL is operating. A 10 kW load is fed from a 220 V AC source operating at a frequency of 50 Hz. By controlling the duty cycle of the SSFCL circuit, the magnitude of the fault current is controlled. Fig. 4 shows the structure of the simulation circuit, and Table I summarizes the circuit parameters used in simulation based on a Matlab/Simulink environment.

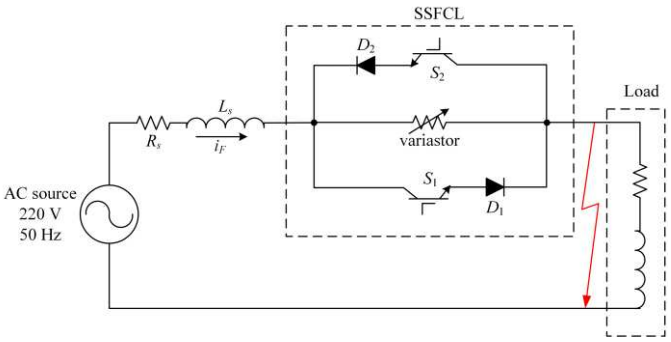

Fig. 6. The structure of simualtion circuit.

Fig. 7 shows the measured load current in three different modes. During the period (0 s ≤ t ≤ 0.1 s), the system operates under normal conditions, both switches conduct for only half cycle separately. At t = 0.1 s, the short circuit is applied and the current flowing through S_1 and S_2 increases. At t = 0.2 s, the switches were controlled with an arbitrary 50 % of duty cycle, leading to a reduction in the rms value of the fundamental component of the fault current.

Fig. 8 shows the measured current for different duty cycles. It is clear that the rms value of the fundamental component of the fault current decreases as the duty cycle decreases. Table II summarizes these values for different values of the duty cycle. Fig. 9 shows the measured fault current at different fault resistances. It is clear that the rms value of the fundamental component of the fault current decreases as the R_F increases. Table III summarizes these values at different values of R_F.

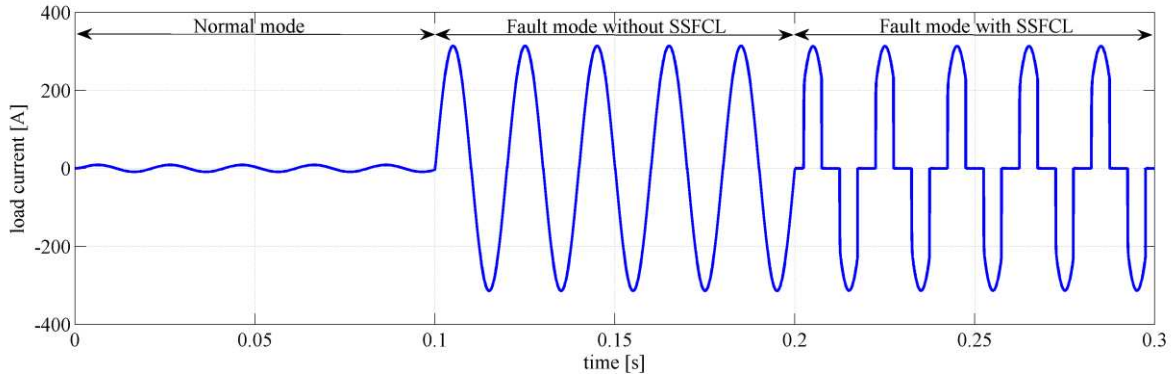

Fig. 7. The measured current under normal condition and under fault condition with/ without aplying the proposed SSFCL.

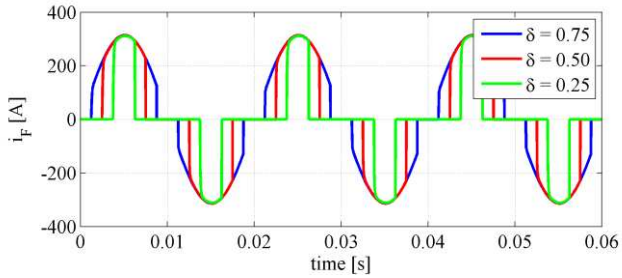

Fig. 8. The measured fault current for different duty cycles.

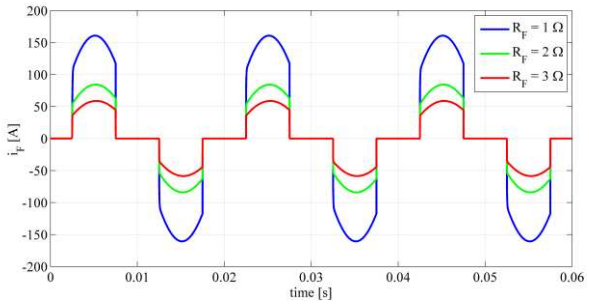

Fig. 9. The measured fault current at different fault resistances.

TABLE I
CIRCUIT PARAMETERS USED FOR SIMULATION

Load active power	P	10 kW
Load power factor	cosφ	0.9
Nominal AC rms voltage	V_n	220 V
Nominal rms current	I_n	50 A
Nominal frequency	f_n	50 Hz
Control time step	T_s	5 µs

TABLE II
THE RMS VALUES OF $I_{F,1}$ FOR DIFFERENT DUTY CYCLES

δ	$I_{F,1,rms}$ [A]
0.75	216.3747
0.50	180.3122
0.25	103.2376

TABLE III
THE RMS VALUES OF $I_{F,1}$ FOR DIFFERENT FAULT RESISTANCES

R_F [Ω]	$I_{F,1,rms}$ [A]
1	127.845
2	48.3661
3	33.5876

IV. CONCLUSION

In this paper, a new control scheme for the SSFCL circuit has been presented. The control method is based on controlling the duty cycle of the switches to limit the rms value of the fundamental component of fault current. Numerical simulations confirm the technical features of the presented control method of SSFCL. The simulation results were conducted by using the Matlab/simulink software, which show the ability of proposed control scheme to limit the peak value of the fundamental component of fault current without affecting the utility voltage and current at normal conditions. This is achieved by controlling the duty cycle of the solid state switches considering the effect of fault resistance; the decrease in the duty cycle and/or the increase in the fault resistance caused a decrease in fault current. However, controlling the duty cycle is better than changing the fault resistance because it is easier to implement, and the resistance could cause more losses in the system.

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