

Design and control of battery charger for electric vehicles using modular multilevel converters

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Abstract

Double-star modular multilevel converters with embedded battery cells are a ground breaking technology for the power converter of electric vehicles. In this topology, the battery cells are connected in series via half bridge DC–DC buck converter and can be independently discharged and recharged. This paper proposes a novel control system for this converter topology that can charge the battery cells from the grid at unity power factor and instantaneously balance them in terms of their state of charges without affecting the grid voltages and currents. The grid current controller is designed and implemented in the stationary reference frame using a proportional-resonant controller, while the state of charge balancing algorithm is designed using sorting algorithm and circulating current control. The simulation and experimental results have demonstrated that the proposed control strategy can effectively charge the battery cells with a negligible distortion of the grid current and can ensure the balance of cells during the recharge without affecting the grid current.

1 | INTRODUCTION

Zero emission electric vehicles (EVs) are an attractive alternative to conventional internal combustion vehicles due to the increase of fuel price in the world and the effect of CO₂ emissions on the environment. However, a significant step for the widespread use of EV could be achieved with light, compact, flexible and reliable power conversion systems that fully meet the high expectations of end customers [1].

At present, the power converters used in Battery Electric Vehicles (BEVs) are traditional 2-level voltage-source inverters. The DC link of the inverter is connected to the battery pack, which consists of a series connected low voltage cells to reach the required DC voltage [2]. Due to the series connection of the cells, the charging and discharging process causes a state of charge (SOC) imbalance, as cells have different leakage currents and electrochemical characteristics; this may damage the cells and reduce their lifetime [3]. For this reason, a battery management system (BMS) is used to balance the cells by shifting the energy from the cells with highest SOC to the cells with lowest

SOCs [3, 4]. However, the BMS increases the size and cost of the BEV, and reduces the efficiency of the conversion system [4]. Additionally, the output waveform of a 2-level inverter has a significant harmonic content. Therefore, the inverter can be used also for battery charging only if passive L or LCL bulky filters are added between the converter and the grid [5]. Also, the converter does not allow single-phase or DC charging [5].

A variety of BMSs can be found in the literature to be used with the 2-level inverter in BEVs to balance the series connected cells during both charging and discharging modes. The topologies are classified according to the active element used for storing the energy such as capacitors, inductors, transformers, or converters [6].

Switched capacitor (SC) and single switched capacitor (SSC) balancing methods have been introduced in [7–10]. They require simple control strategy to balance the cells and can work in both recharging and discharging modes. However, they have a relatively long balancing time and intelligent control is necessary to fast the equalization. A Double-tiered switched capacitor (DTSC) balancing method has been proposed in [11] to reduce

the balancing time to a quarter of the time required for balancing the cells using the switched capacitor method, but it is implemented with high number of switches.

Multi-winding transformer (MWT) and multi-switched inductor (MSI) balancing methods have a faster balancing speed compared to the capacitor-base balancing methods. However, these topologies are not suitable for Li-ion batteries because they balance the cells by sensing the voltage differences between cells. Moreover, they use a high number of inductors and iron cores, so they have the largest sizes and high magnetic losses [12–15]. On the other hand, single winding transformer (SWT) and a single switch inductor (SSI) have faster balancing speed and lower magnetic losses, but they require complex control strategy to balance the cells. To add one or more cells to SWT, the core must be changed. In addition, since the switching frequency is quite high, extra filtering capacitors are needed for SSI topology across each battery cell to filter the high frequency harmonics [16–18].

The bi-directional Ćuk converter has been reported in [19] and [20] as an active cell balancing topology. It transfers the energy between two adjacent cells, so it will take a relatively long balancing time especially for a long string of battery pack. Buck-boost converter (BBC) and full bridge converter (FBC) balancing methods have been proposed in [21–23] and they are widely used in cell balancing systems because they have the fastest balancing speed with acceptable energy losses, but they require complex control strategy to balance the cells. These topologies are relatively expensive and complex but they are suitable for modular design with high efficiency. A Flyback converter (FbC) balancing method has been introduced in [24, 25] and it is widely used in EV applications because it is suitable for modularized system with a satisfactory equalization speed. Drawbacks are the uniformity of the multi-winding as well as the magnetic losses. A ramp converter (RC) has been proposed in [26] as an active cell balancing method. This topology requires half the number of secondary windings compared to MWT method and provides a soft switching along with a relatively simple transformer. However, it requires complex control and has a satisfactory balancing speed. A quasi-resonant converter (QRC) has been proposed in [27] and [28] as a balancing method. The main advantage of this topology is that, it can reduce the switching losses thus increasing the balancing system efficiency with satisfactory equalization speed. However, it has very complex control, difficult implementation, as well as a high cost. A non-isolated DC/DC-converter and a switch-matrix have been proposed in [29] as a new approach to active charge balancing in Lithium-ion battery systems. This method can balance the cells quickly with acceptable energy losses, but it requires complex control strategy to balance the cells.

The Cascaded H-Bridge Converter (CHB) with embedded batteries has been proposed in [30] as an application for high power Hybrid Electric Vehicles (HEVs) motor drives. The converter consists of a set of star-configured converter legs in which the AC sides of multiple H-bridge converters are cascaded to constitute each leg. The converter is able to balance the batteries quickly, but it is implemented with a high number of switches and has low reliability when full power is required. This topol-

ogy allows the recharging of batteries only from a three-phase AC source.

Double Star Modular Multilevel Converter (DS-MMC) with embedded battery cells has been proposed in [31–35] as a variable speed drive for traction motors of EVs. The DS-MMC drives the traction motor and instantaneously balances all the battery cells in terms of their state of charges without affecting the motor voltages and currents. The use of this converter eliminates the need for the traditional BMS since it is replaced by the control of the converter. This topology has many advantages compared to the present power conversion systems of BEVs:

- (i) The output waveforms have very low harmonic content, which simplifies the requirement of filters design.
- (ii) The topology is redundant, i.e. if one cell is damaged, the whole leg still works at lower maximum voltage.
- (iii) Additional modules can be easily added in a modular arrangement in case of increased output voltage.
- (iv) The modularity design makes the converter more flexible on the SOC balance between the battery cells.
- (v) The converter can run at a very low switching frequency or even with nearest-level modulation, which results in reduced switching losses.
- (vi) This topology allows the recharging of electrochemical cells either from DC or AC power sources (single-phase or three-phase).

The authors have already proposed in [31] a Modular Multilevel Converter with embedded battery cells as a variable speed drive for traction motors of EVs. This paper is an extension of our previous work as there is no previous research on design and control of the recharge process using this converter topology at unity power factor. This paper addresses this gap by modelling, simulating and implementing a grid current controller in the stationary reference frame (*abc* domain) without the need for *dq* frame transformation to accommodate for unbalanced and distorted grid voltages. The main contribution of the paper is to highlight the capabilities of the proposed converter with embedded battery cells for the use with electric vehicles as a battery charger with a fast SOC balancing during the recharge process. The grid power controller is combined with SOC balancing algorithm to charge battery cells of a DS-MMC from a three-phase AC grid at a unity power factor. The paper shows that DS-MMC does not require grid filters since it generates an output voltage with a negligible distortion. The control system allows the converter to use the grid current to balance the battery cells very quickly without affecting the balancing of grid current. The current control has been designed in the stationary frame using proportional resonant (PR) controllers as they are less affected by imbalance and distortion of the grid voltage [36].

The rest of the paper is organised as follows: Section 2 introduces the structure and the operation principle of the DS-MMC and includes the mathematical model to design the charge control system of the converter. Section 3 describes the SOC balancing control and the grid power control. Sections 4 and 5 present simulation and experimental results on a kW-size

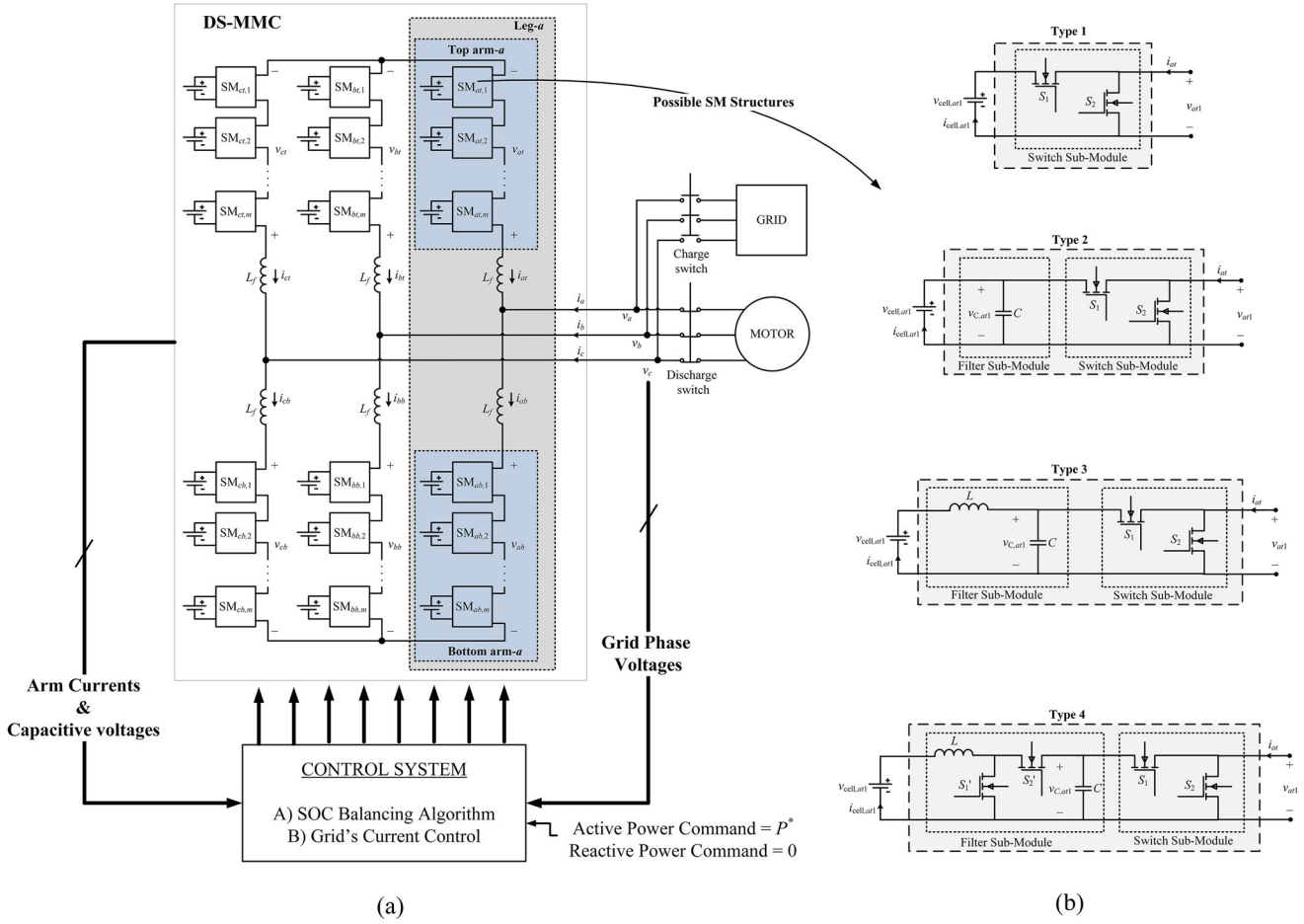


FIGURE 1 (a) A block diagram of the conversion system, (b) Possible SM structures

prototype for the charge control algorithm, respectively. Section 6 compares between the proposed converter configuration and alternative configurations with CHB and two-level inverter for different active cell balancing topologies. Section 7 presents the drawbacks of the converter when it is fitted in a real vehicle and discusses some possible solutions. The last section is the conclusion of the work and recommendation for future research.

2 | DOUBLE STAR-MODULAR MULTILEVEL CONVERSION SYSTEM

The block diagram of the whole system with the conversion system is shown in Figure 1. The system can operate either in a discharging or a charging mode. In the discharging mode, the DS-MMC drives a three-phase AC motor and instantaneously balances all the battery cells within each arm, in terms of their SOC. In this mode, the converter control system consists of an SOC controller and motor speed controller. The primary objective of an SOC audit is to provide transparency related to a service organization's internal control structure. In the charging mode, which is the focus of this paper, the DS-MMC is connected to the grid via the charge-

ing switches to charge the battery cells. The converter is controlled using decoupled active and reactive power control system, which is able to recharge the battery cells at unity power factor. This controller is combined with the SOC-balancing controllers to balance the battery cells during the charging mode. The grid frequency and phase angle are estimated using a phase-locked loop (PLL) algorithm. Figure 2 shows the equivalent circuit of the DS-MMC, when it is connected to the grid.

The converter consists of three legs, where each leg consists of two arms (top and bottom arms). Each arm consists of m cascaded connected sub-modules (SMs), such that each SM consists of filter SM and switch SM. The block diagram of the possible SM structures for the MMC converter with embedded battery cell is shown in Figure 1. Most common topologies (four types) are given for each block and will be explained in the text below where each type offers different advantages and disadvantages. Comparisons between different types of SMs are given in Table 1:

- (i) Type 1: The battery cell is connected directly to the switch SM without filtering out the cell's current [31, 32]. In this case, the cell's current goes from zero to arm current depending on whether the SM is bypassed or inserted into

Equivalent circuit of DS-MMC

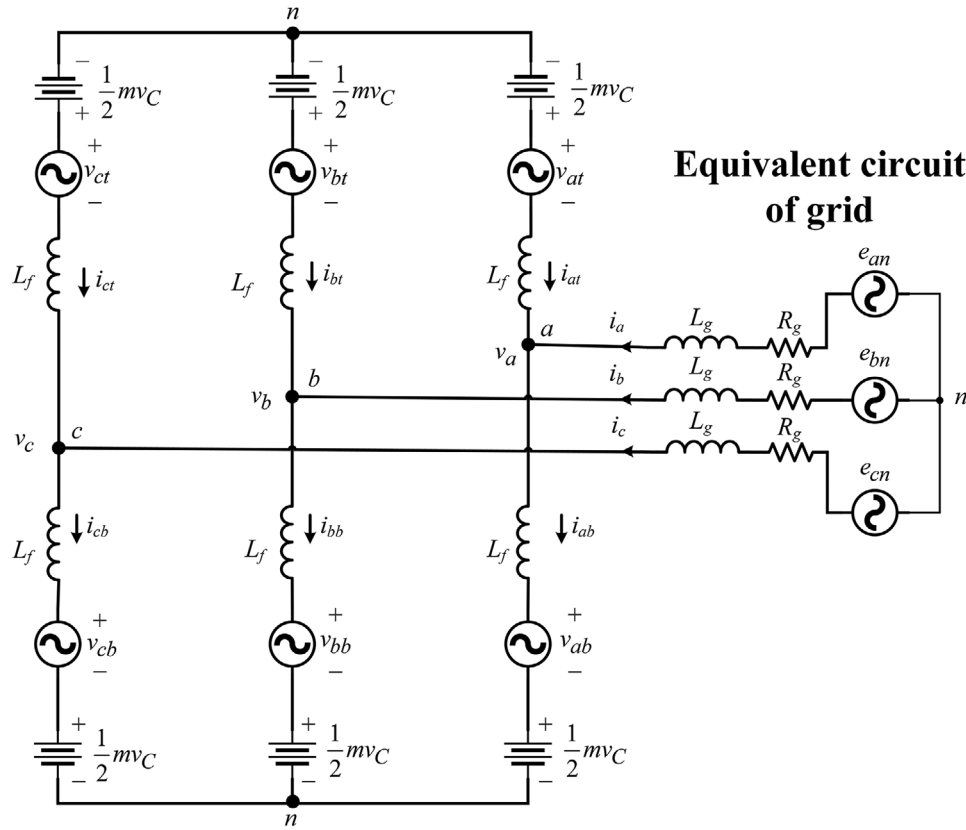


FIGURE 2 The equivalent circuit of the proposed system

TABLE 1 Comparison between different types

	Type 1	Type 2	Type 3	Type 4
Harmonic content of cell's current	High	Very small	Very small	Very small
Dominant AC Component in the cell's current	High	High	High	Very small
Harmonic Content of motor's current at low frequency	Eliminated	High	High	High
Number of capacitors	0	$6m$	$6m$	$6m$
Number of inductors	6	6	$6m + 6$	$6m + 6$
Number of MOSFETs	$12m$	$12m$	$12m$	$24m$
Complexity of the converter	Good	Good	Good	Satisfactory
Converter reliability	Excellent	Very good	Good	Satisfactory
Converter efficiency	Good	Good	Good	Satisfactory
Battery lifetime	Satisfactory	Good	Good	Excellent
Converter Cost	Very good	Good	Satisfactory	Satisfactory

the string of cells creating the arm voltage. Therefore, the cell's current will have high harmonic content and dominant AC components at f_1 and $2f_1$ frequencies, as shown in Figure 3, where f_1 is the fundamental frequency. This current may eventually deteriorate the cell and cause unnecessary losses making the DS-MMC inefficient. However, this

type is capable of running constant-torque loads from zero up to the nominal motor speed without any need for additional current capability since there is no passive elements used within each SM in the converter.

- (ii) Type 2: In this type, a shunt capacitor is connected to the battery cell as a filter to reduce the harmonic content of

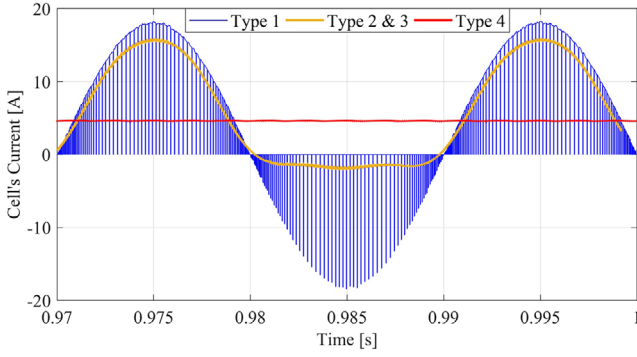


FIGURE 3 Typical cell charging currents for different SM topologies

the cell's current. The capacitor and internal resistance of the cell will form RC filter between the switches and the cell, which is able to absorb some of the higher harmonics in the cell's current. This type is also capable of running constant-torque loads from zero up to the nominal motor speed without any need for additional current capability.

- (iii) Type 3: In this type, an inductor is added in series with the cell. The inductor, internal resistance of the cell, and the shunt capacitor will form RLC filter, which is able to filter out the harmonic contents in the cell's current. The size of the capacitor and the inductor is determined by the RMS value of the AC current components flowing into the cell. In this type, super-capacitors should be used to reduce the ripple voltage within each SM at low frequency operation of traction motor.
- (iv) Type 4: In this type, additional boost converter stage is used as an active filter to eliminate the harmonic content of the cell's current with its dominant AC component with boosting capabilities. However, it introduces additional losses on the added switching elements and makes the whole converter even more complex. The main drawback of using buck-boost filter module is decreased converter reliability as a result of two additional switches introduced in each cell, and the need for super-capacitors to reduce the ripple voltage within each SM at low frequency operation in the motoring mode.

The RC filter module shown as Type 2 is chosen for the analysis, modelling, and implementation in the current paper to reduce the complexity of the converter, increase the reliability of the converter, and avoid using super-capacitors.

In each SM, only one switch is turned on at a time to avoid the short circuit across the battery cell. When S_1 is switched on, the SM voltage is the battery cell voltage, v_{cell} , and the cell is charged if the arm current is positive and discharged if it is negative. When the switch S_2 is turned on, the SM voltage is zero and the cell state is unchanged. The SM rated voltage is equal to the nominal cell voltage. Therefore, low voltage MOSFETs can be used in this converter instead of IGBTs to reduce conduction and switching losses.

If the number of SMs within each arm is m , the line-to-line output voltage of the converter has $m + 1$ levels. As the output voltage on each SM is either v_C or zero, the maximum voltage across each arm is $m \times v_C$. The high number of output levels gives a low total harmonic distortion (THD), and thus no need of filters for the connection to the grid.

The current flowing through one arm is the same current flowing through the battery cell when the corresponding SM is turned on (S_1 is on and S_2 is off). The direction of the cell's current then determines the mode of the cell (charging or discharging).

In this paper, all the quantities referred to phases a , b and c are denoted with the subscript abc . Quantities associated to the top and bottom arms are indicated with the subscripts t and b , respectively.

The vectors of the top and bottom arm currents, $i_{abc,t}$ and $i_{abc,b}$, of the phases a , b , and c can be expressed as:

$$\underbrace{i_{abc,t}}_{[i_{at} \ i_{bt} \ i_{ct}]^T} = i_{abc,cir} - \frac{1}{2}i_{abc}; \quad \underbrace{i_{abc,b}}_{[i_{ab} \ i_{bb} \ i_{cb}]^T} = i_{abc,cir} + \frac{1}{2}i_{abc} \quad (1)$$

where $i_{abc,cir}$ is the circulating current vector and i_{abc} is the grid's current vector.

Using the equivalent circuit of the converter in Figure 2, The voltage of the top and bottom arms, $v_{abc,t}$ and $v_{abc,b}$, of the phases a , b , and c , in the hypothesis of balanced cells, can be expressed as:

$$v_{abc,t} = \frac{1}{2}mv_C - v_{abc} - v_{L,abc,t}; v_{abc,b} = \frac{1}{2}mv_C + v_{abc} - v_{L,abc,b} \quad (2)$$

where v_{abc} is the grid voltage vector with respect to the neutral point, n , $v_{L,abc,t}$ and $v_{L,abc,b}$ are the voltage drop vectors across top and bottom buffer inductors, L_f , which are given by:

$$v_{L,abc,t} = v_{L,cir,abc} - v_{L,abc}; v_{L,abc,b} = v_{L,cir,abc} + v_{L,abc} \quad (3)$$

$$v_{L,cir,abc} = L_f \frac{di_{cir,abc}}{dt}; \quad v_{L,abc} = \frac{1}{2}L_f \frac{di_{abc}}{dt}$$

The converter is modulated using a carrier disposition-third harmonic injection PWM (CD-THIPWM), which has a superior performance in respect of reduced harmonic current ripple and increased voltage transfer ratio compared to other modulation schemes such as a carrier disposition sinusoidal PWM (CD-SPWM) and a phase shifted carrier-sinusoidal pulse width modulation (PS-SPWM) schemes.

Figure 4 illustrates the CD-THIPWM scheme to run the top and bottom arms, where a third-harmonic component is injected to the modulating waves to increase the maximum peak value of the converter phase voltage with respect to the motor or grid neutral point without causing an over-modulation. The vectors of modulating waves for bottom and top arms, $v_{abc,b}^*$

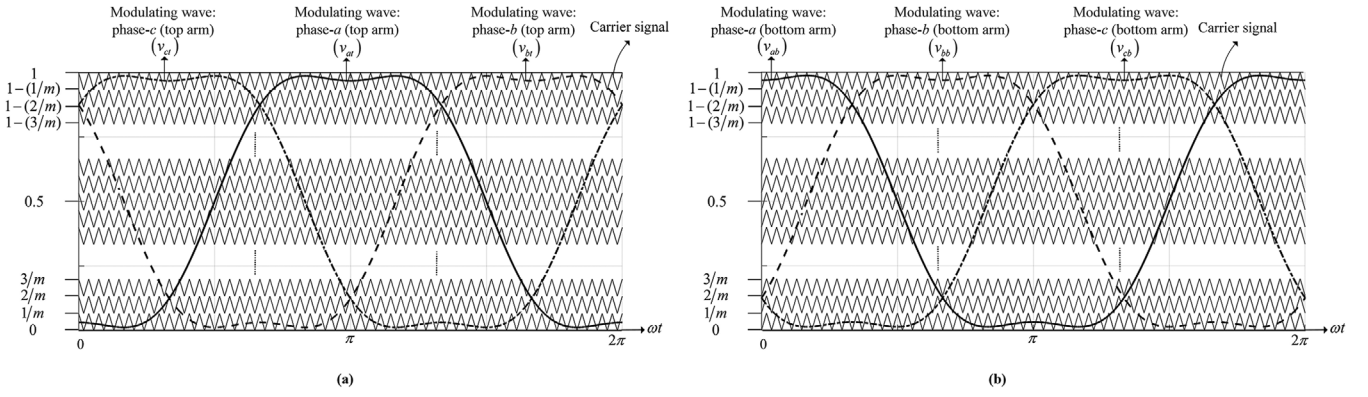


FIGURE 4 A CD-THIPWM scheme for: (a) Top arms, (b) Bottom arms

and $v_{abc,t}^*$, can be expressed by:

$$\begin{aligned} v_{abc,t}^* &= \frac{1}{2}mv_C - v_{L,abc,t} - M \sin(\theta + \chi_{abc}) - \frac{1}{6}M \sin(3\theta); \\ v_{abc,b}^* &= \frac{1}{2}mv_C - v_{L,abc,b} + M \sin(\theta + \chi_{abc}) + \frac{1}{6}M \sin(3\theta); \end{aligned} \quad (4)$$

$$\theta = \omega t + \phi_v; \quad \chi_{abc} = \begin{bmatrix} \chi_a \\ \chi_b \\ \chi_c \end{bmatrix} = \begin{bmatrix} 0 \\ +2\pi/3 \\ -2\pi/3 \end{bmatrix},$$

where ω is the electric angular frequency of the modulating waves, ϕ_v is the phase angle of the modulating wave or the grid phase voltage, and M is the modulation index of the converter, which is given by:

$$M = \frac{2V_m}{mv_C}; \quad 0 \leq M \leq \frac{2}{\sqrt{3}} \quad (5)$$

where V_m is the peak value of the grid's phase voltage (North American standard voltage, $V_m = 120\sqrt{2}$) and v_C is the capacitive or cell voltage.

The modulating waves of both top and bottom arms are estimated based on current and SOC controllers and then compared with the carrier signals to determine the number of active SMs in each arm. Each carrier has a peak-to-peak voltage of $1/m$ and a switching frequency of f_{sw} . The carriers are shifted vertically by $1/m$ in the range of 0 to 1.

In the BEVs, Li-ion battery cells are widely used because they have high energy density compared with nickel-cadmium, nickel metal hybrid and Lead acid battery cells. The SOC of the cell gives an indication on its residual capacity. The SOC is defined as the ratio of the available capacity of the battery to its maximum available capacity, and it can be estimated using the Coulomb-counting method as [37]:

$$\text{SOC} = \frac{Q - q}{Q} = \text{SOC}_i - \frac{1}{3600 Q} \int i_{\text{cell}} dt, \quad (6)$$

where q is the charge absorbed from the cell in [Ah] and Q is capacity of the cell in (Ah), SOC_i is the initial SOC of the cell

in (%), and i_{cell} is the current supplied by the cell in (A). In this paper, the Li-ion cells are modelled during the discharge and recharge modes using battery dynamic model for EV applications given in [38]. In this model, the temperature and self-discharging effects are ignored, the internal resistance and the capacity of the cell are assumed to be constant and independent of the cell current.

3 | CONTROL SYSTEM OF THE CONVERTER

The DS-MMC is intended to have the function of battery charger when the traction motor is disconnected from the converter via the interlocked contactors. Figures 5 and 6 show the proposed control system of the converter, when it is connected to the grid for charging purposes. The control system consists of two controllers: SOC balancing controller and grid current controller. The detailed operation of each controller is considered in the next subsections.

3.1 | SOC balancing controller

The function of SOC balancing controller is to balance all battery cells in each converter arm. In order to balance the SOC of the cells, the following algorithm is applied for each arm [31, 32]:

- (i) The top and bottom arm currents, $i_{abc,t}$ and $i_{abc,b}$ are measured using accurate current sensors, (six arm currents).
- (ii) The current flowing into or out of each cell is estimated using the measured arm current, and the gate signal of the switch S_b as follows (Measuring all the cell currents is not necessary):

$$[i_{abc,t,b} \ i_{abc,b,b}] = \begin{cases} [i_{abc,t} \ i_{abc,b}], & \text{when } b\text{-th SM is ON} \\ [0 \ 0], & \text{when } b\text{-th SM is OFF} \end{cases} \quad (7)$$

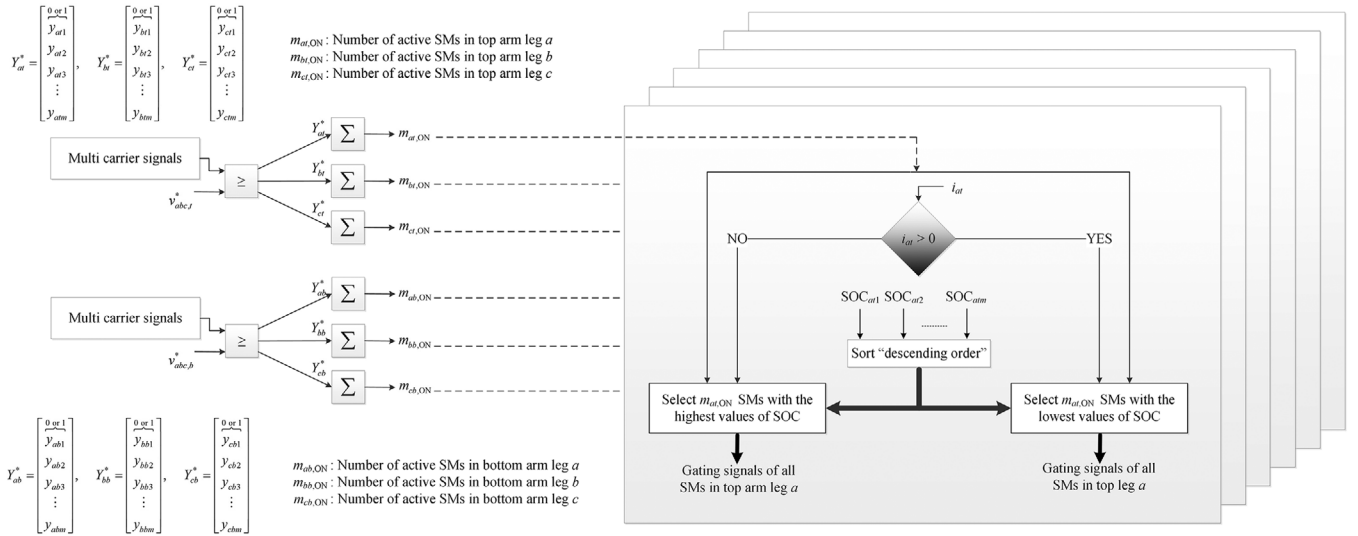


FIGURE 5 A block diagram of SOC balancing controller

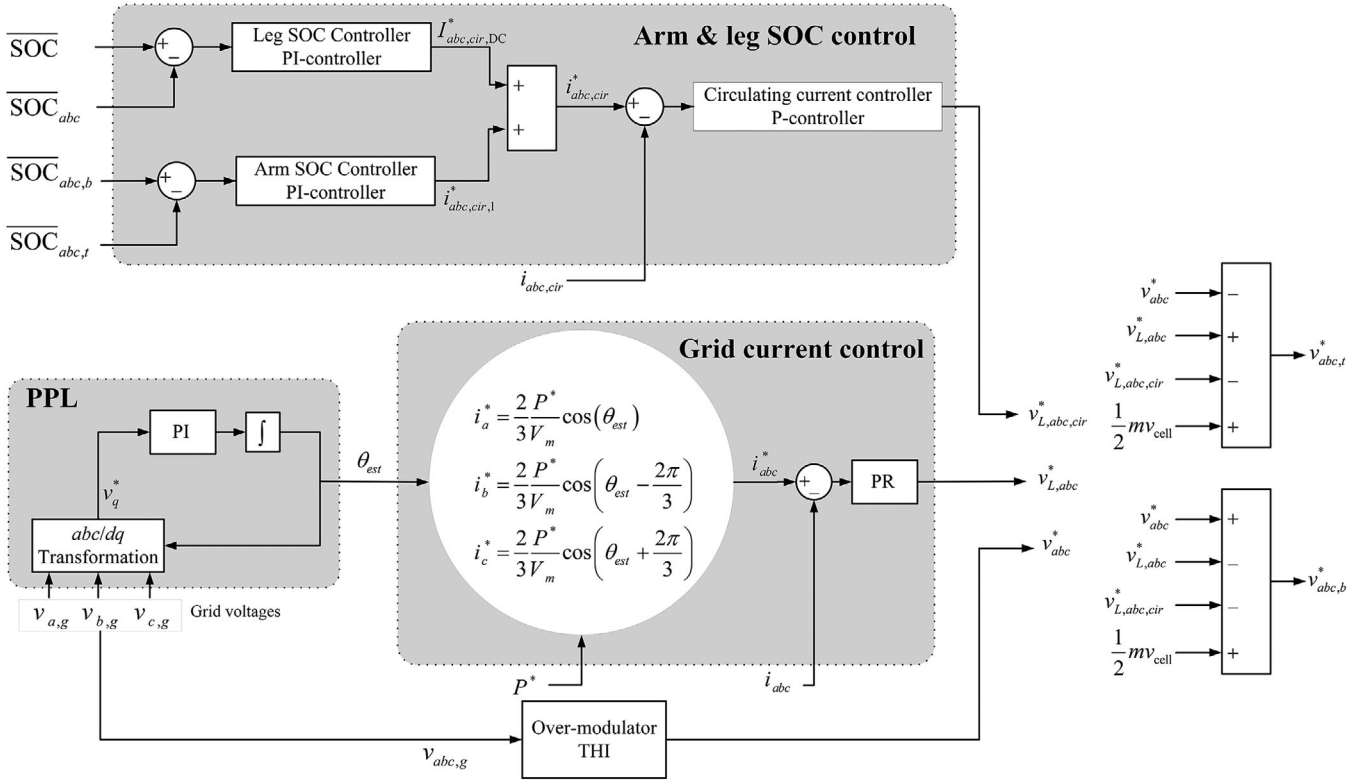


FIGURE 6 A block diagram of the circulating current controller with the proposed grid's current controller

- (iii) The SOC of the cells are estimated every millisecond using the Coulomb-counting method (given in (6)).
- (iv) The number of active SMs within each arm is determined as follows:

For the top arm of phase- a , the modulating wave, v_{at} , is compared with m carrier signals, and the output of com-

parison is a binary array, Y_{at}^* , of size $m \times 1$, which is given by:

$$Y_{at}^* = \begin{pmatrix} \underbrace{y_{at1}}_{0 \text{ or } 1} & \underbrace{y_{at2}}_{0 \text{ or } 1} & \underbrace{y_{at3}}_{0 \text{ or } 1} & \cdots & \underbrace{y_{atm}}_{0 \text{ or } 1} \end{pmatrix}^T \quad (8)$$

and the number of active SMs, $m_{at,ON}$, is the number of ones in Y_{at}^* . For example, if the binary representation of Y_{at}^* is 1000 for $m = 4$ SMs, then the number of active SMs is 1. Similarly, if the binary representation of Y_{at}^* is 1011, then the number of active SMs is 3. The number of active SMs in the other arms are determined by the same way.

- (v) The cells are sorted in a descending order according to their SOC.
- (vi) When the arm current is discharging the battery cells in the arm, the active cells with the highest SOC are switched-on.
- (vii) In the next half cycle of arm current, the cell current becomes negative and the cell operates in charging mode. In this case, the active cells with the lowest SOC are selected to be switched on.

Using this method, SOC balancing is guaranteed within the arm and all cells will have the same SOC, which is equal to the moving average SOC of that arm. Figure 5 summarises the procedure necessary to achieve the SOC balancing strategy with each arm of the converter.

The arm and leg balancing control is required to achieve the energy balance between the top and bottom arms and between the three legs of the converter. The balance is attained by injecting a circulating current, $i_{abc,cir}$, to the converter. This current must be able to transfer the power from the arm with highest average SOC to the arm with lowest average SOC within the same leg and instantaneously transfer the power from the leg with highest average SOC to the leg with lowest average SOC.

Figure 6 shows the implementation of the arm and leg SOC controller where the output of the arm controller is the vector $i_{abc,cir,1}$, and the output of the leg controller is the vector $I_{abc,cir,DC}$. By ignoring the switching losses and the ripples due to the AC power components and considering the voltage drop across buffer inductors, the vectors of the differential and total instantaneous power, Δp_{abc} and Σp_{abc} , are given in Equation (9) where:

- (i) $I_{abc,cir,1}$ is the magnitude's vector of the fundamental components of circulating currents,
- (ii) $\beta_{abc,cir,1}$ is the phase angle vector of the fundamental components of circulating currents,
- (iii) $I_{abc,cir,DC}$ is the magnitude's vector of the DC components of circulating currents,
- (iv) I_m is the peak value of the grid current,
- (v) ϕ is the grid power factor's angle,
- (vi) $v_{L,abc,cir}^*$ is the voltage drop required to achieve the balance the converter arms and legs.
- (vii) $F = 2Q/M$, $G = 1/(4Q)$,
- (viii) ζ_1, ζ_2 are the damping ratios,
- (ix) ω_{n1}, ω_{n2} are the natural frequencies,

- (x) and τ is the time constant of the circulating current controller. <?TeX

$$\begin{aligned}
 \Delta p_{abc} &= m Q v_{cell} \frac{d}{dt} \left[\overline{\text{SOC}}_{abc,t} - \overline{\text{SOC}}_{abc,b} \right] \\
 &\approx -V_m I_{abc,cir,1} \cos \beta_{abc,1} \Rightarrow \frac{\overline{\text{SOC}}_{abc,b} - \overline{\text{SOC}}_{abc,t}}{\overline{\text{SOC}}_{abc,b} - \overline{\text{SOC}}_{abc,t}} \\
 &= \frac{k_1}{F} \frac{s + k_2/k_1}{s^2 + (k_1/F)s + (k_2/F)} \\
 &\quad \frac{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} \\
 \Sigma p_{abc} &= 2m Q v_{cell} \frac{d\overline{\text{SOC}}}{dt} \\
 &\approx \underbrace{\frac{1}{2} m v_{cell} I_{abc,cir,DC}}_{\text{Power required to balance the three legs}} + \underbrace{\frac{1}{2} V_m I_m \cos(\phi)}_{\text{Power delivered by the grid}} \\
 \Rightarrow \frac{\overline{\text{SOC}}}{\overline{\text{SOC}}} &= \frac{k_3}{G} \frac{s + k_4/k_3}{s^2 + (k_3/G)s + (k_4/G)} \\
 &\quad \frac{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} \\
 v_{L,cir,abc} &= L_f \frac{di_{abc,cir}}{dt}; \text{ where } i_{abc,cir}^* = I_{abc,cir,DC} \\
 &+ \underbrace{I_{abc,cir,1} \sin(\theta + \chi_{abc} + \beta_{abc,1})}_{i_{abc,cir,1}} \Rightarrow \frac{I_{abc,cir}}{I_{abc,cir}^*} = \frac{1}{s(L_f/k_5) + 1} \quad (9)
 \end{aligned}$$

3.2 | Grid's current controller

The function of the grid's current controller is to charge the battery cells from the grid at unity power factor. The converter is connected to the three-phase AC grid and the current must be controlled using a PLL to obtain unity power factor operations. The block diagram of the charging process of the battery cells with the PLL and charging controller is shown in Figure 6. The PLL is implemented using a dq -transform with an appropriate loop filter. The transfer function of the PLL is given by [39]:

$$\begin{aligned}
 \frac{\Theta_{est}}{\Theta} &= (-V_m k_6) \frac{s + k_7/k_6}{s^2 - (V_m k_6)s - (V_m k_7)}; \\
 \Theta &= \mathcal{L}^{-1}(\Theta) = \int \omega dt; \Theta_{est} = \mathcal{L}^{-1}(\Theta_{est}) \quad (10)
 \end{aligned}$$

where

- (i) Θ and Θ_{est} are the actual and estimated grid's phase angles in s -domain, respectively.
- (ii) θ and θ_{est} are the actual and estimated grid's phase angles in t -domain, respectively.
- (iii) ω is the radian frequency of the grid.
- (iv) $\mathcal{L}^{-1}$ is the inverse Laplace operator.

Based on the estimated angular position of the grid via the PLL, the reference grid currents, i_{abc}^* are calculated as:

$$i_{abc}^* = \frac{2}{3} \frac{P^*}{V_m} \sin(\theta_{est} + \chi_{abc}); \quad (11)$$

where P^* is the power delivered from the grid for charging the battery cells. The grid voltages are measured by voltage sensors and the PLL algorithm yields the phase angle of the grid voltages, θ_{est} .

In the grid current controller, The reference grid currents, i_{abc}^* , are generated using Equation (11). They are compared with the measured grid currents, i_{abc} , to produce the current error signal for the PR current controller, which acts on the current error to produce the voltage references for the three-phase voltages, $v_{L,abc}^*$. The grid phase voltages are measured and then added to the third harmonic component to produce v_{abc}^* . The final modulating waves for the top and bottom arms are generated using (4), which are then used by the CD-THIPWM modulator to generate the appropriate pulses for the switches of the SMs. Figure 6 shows the implementation of the grid current controller, which is designed using the term $v_{L,abc}$ in Equation (3):

$$\underbrace{v_{L,abc} = \frac{1}{2} L_f \frac{di_{abc}}{dt}}_{\text{time-domain}} \xrightarrow{c} \underbrace{V_{L,abc} = \frac{1}{2} L_f s I_{abc}}_{\text{s-domain}} \quad (12)$$

The transfer function of the proposed current controller is given by:

$$\frac{I_{abc}}{I_{abc}^*} = \frac{G_{PR}(s) G(s)}{1 + G_{PR}(s) G(s)}; \quad G(s) = \frac{I_{abc}}{V_{L,abc}} = \frac{2}{L_f s} \quad (13)$$

where $G_{PR}(s)$ is the transfer function of the PR block in the current controller, which is given by:

$$G_{PR}(s) = \frac{V_{L,abc}}{E} = \frac{V_{L,abc}}{I_{abc}^* - I_{abc}} = k_8 + k_9 \frac{s}{s^2 + \omega^2} \quad (14)$$

and the resonant term, $k_9 s/(s^2 + \omega^2)$, is represented in the state space using the controllable canonical form as:

$$\begin{aligned} dx/dt &= Ax + Bu; y = Cx \\ x &= \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, A = \begin{bmatrix} 0 & 1 \\ -\omega^2 & 0 \end{bmatrix}, B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, C = [0 \ k_9] \end{aligned} \quad (15)$$

where x_1 and x_2 are the state variables for the grid current controller, u is the error current signal and y is the output of the resonant term in the PR control block. This representation can be easily implemented using Matlab/Simulink for simulation and NI CompactRIO (FPGA target) for experiment.

4 | SIMULATION RESULTS

This section shows the main characteristics of the proposed converter with integrated battery cells using Matlab/Simulink numerical simulations. A three-phase, 220 V, and 50 Hz grid is connected to the converter. The grid's line resistance and

TABLE 2 Data of the simulated Li-Ion cell

Parameter	Unit	Value
E_0	V	4.2673
K	V/(Ah)	3.5397×10^{-5}
R	m Ω	2.4557
A	V	0.28621
B	Ah $^{-1}$	4.0708
Q	Ah	7.5

TABLE 3 Control gains of controllers used in simulation

Gain	Value	Control parameters
k_1	47.9831	$\zeta_1 = 35.355, \omega_{n1} = 0.0025 \text{ r/s}$
k_2	0.0017	
k_3	47.9831	$\zeta_2 = 35.355, \omega_{n2} = 0.0013 \text{ r/s}$
k_4	0.00085	
k_5	0.4443	$\tau = 112.5 \mu\text{s}$
k_6	-2.222	$\zeta_3 = 1, \omega_{n3} = 200 \text{ r/s}$
k_7	-222.2	
k_8	0.4443	$\zeta_4 = 7, \omega_{n4} = 1257 \text{ r/s}$
k_9	39.4784	

inductance are assumed to be 150 m Ω and 0.1 mH, respectively. The grid's frequency is assumed to be continuously changing within the limits specified by the electricity supply regulations (i.e. $\pm 1\%$ of nominal grid frequency). The converter has 84 SMs per each arm and 80 cells (3.7 V and 7.5 Ah). The cells are assumed to have different initial SOC between 20% and 50% in each leg with different initial average SOC for the three legs. The cells are charged up with a charging rate of 10 kW, approximately equivalent to a charging rate of 0.715C. Table 2 summarises the data used in the simulated model for the Li-ion cells. The converter is modulated using the THI-SPWM at a switching frequency of 4.05 kHz. Table 3 summarises the control gains used for simulation during the charge mode.

The results in Figure 7 show the responses of the PLL controller when its natural frequency is chosen to be 100 and 200 rad/s, respectively, where the damping ratio of the controller is set to 1 and the peak of the grid phase voltage is 180 V. It is clear that, the PLL controller estimates correctly the angular position of the grid voltage and that a higher natural angular frequency of the controller has a faster dynamic response.

The SOC of all the cells in the three legs and the average SOC of the three legs are shown in Figure 7. It is clear that the cells are totally balanced within about 3000 s by charging more the cells with lower SOC and less the cells with higher SOC. The converter charges up the cells completely within about 4100 s. The three legs are totally balanced within about 2100 s by transferring the energy from the highest average SOC leg to the lowest average SOC leg. The results show the capability of arm,

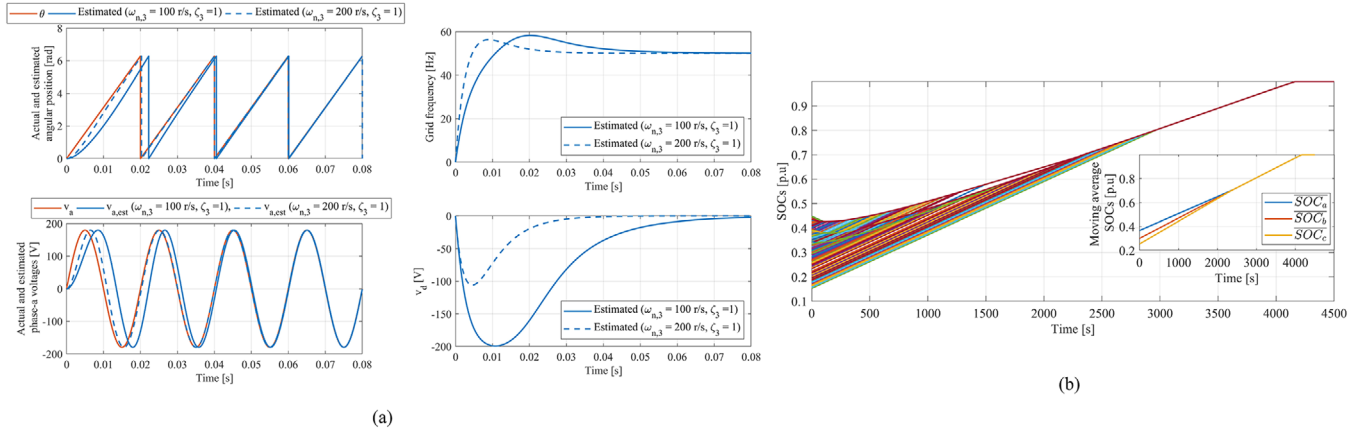


FIGURE 7 (a) The responses of the PLL at natural radian frequencies of 100 and 200 r/s, (b) The estimated SOC

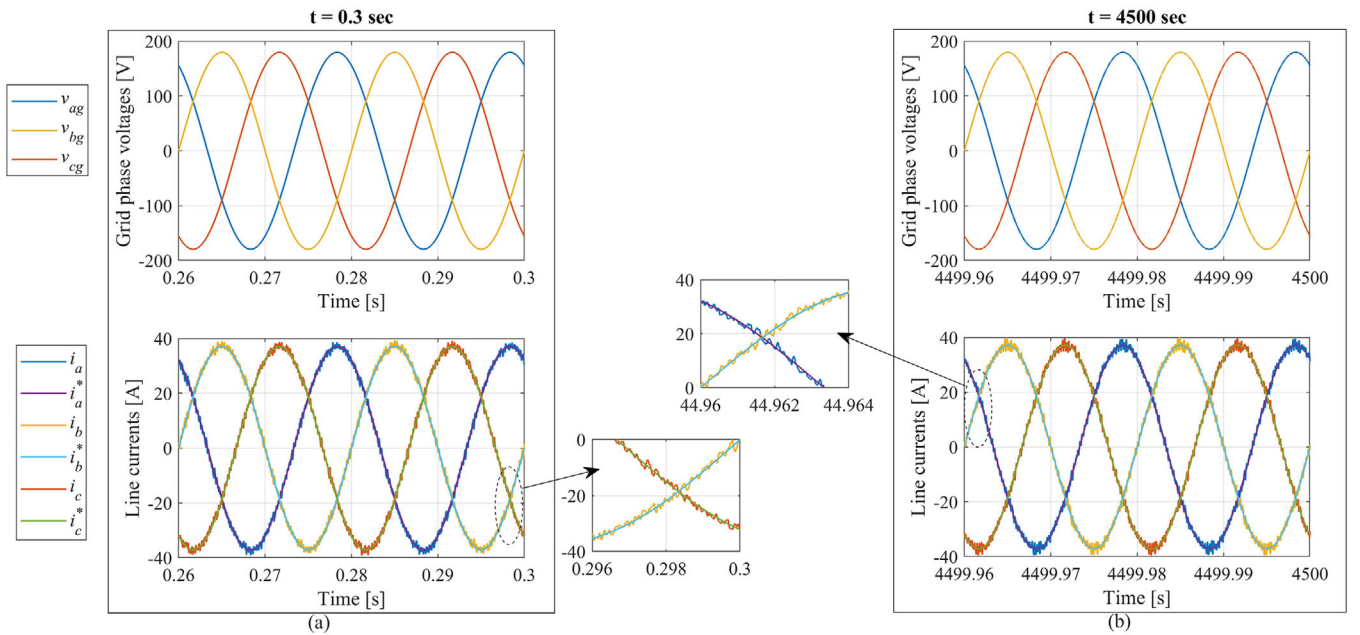


FIGURE 8 The grid's phase voltages and currents with a step reference power of 10 kW at (a) $t = 0.3$ s and (b) $t = 4,500$ s

leg, and single SOC controllers in balancing the battery cells during the charging mode without affecting the operation of grid's current controller.

Figures 8 and 9 present the grid's measured phase voltages, the converter's line-to-line voltages, the reference and measured grid's phase currents, the arm voltages and currents, and the estimated circulating currents when the cells are unbalanced at $t = 0.3$ s and when they are balanced at $t = 4500$ s. It is clear that the current and voltage are in phase and the proposed control system is able to charge the battery cells from the grid at a unity power factor. The converter produces high quality line current, due to the low harmonic distortion of the voltage, which is 0.91%. The PR grid current controller shows a good capability of tracking the reference grid currents even during cell balancing. It is worth noting that the grid phase currents are always symmetrical regardless of the SOC imbalance of

the cells. Since the converter legs and arms have different initial average SOC, the arm and leg SOC controllers inject circulating currents to achieve energy balance between the converter legs and arms, as Figure 9 shows. At steady-state conditions, the converter's legs and arms are balanced, and the injected circulating currents become zero as shown in the same Figure 9.

5 | EXPERIMENTAL RESULTS

The proposed control system has been designed and implemented using NI CompactRIO to verify the correctness of the simulated results. In order to reduce complexity, the DS-MMC has been designed with four SMs per arm, with a voltage of 10 V and current of 50 A. The converter is connected to a 400 V,

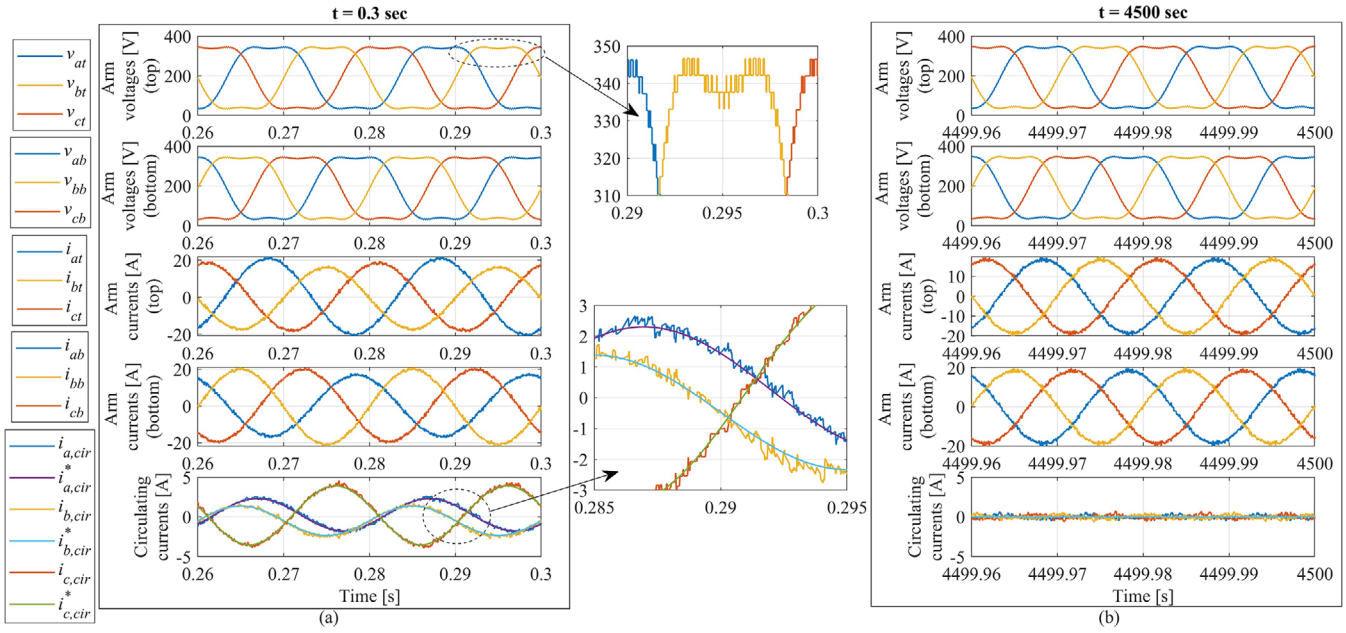


FIGURE 9 The converter arm voltages and currents, and the circulating currents with a step reference power of 10 kW at (a) $t = 0.3$ s and (b) $t = 4,500$ s

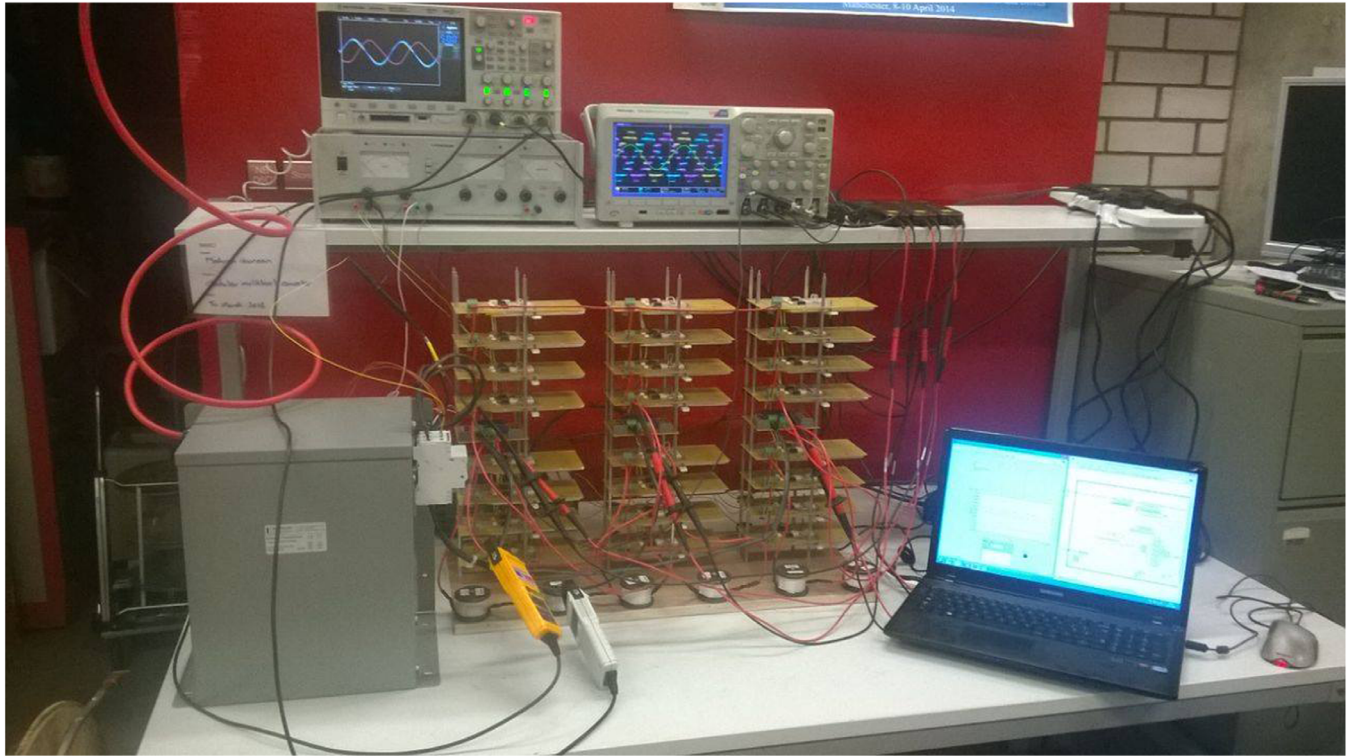


FIGURE 10 A photograph of the prototype system built in the laboratory

50 Hz three-phase grid via a 400 V/10 V, 1.2 kVA three-phase transformer. In this experiment, the converter is modulated using CD-THIPWM with a 2.25 kHz switching frequency. A photograph of the system built in the laboratory is shown in Figure 10. Each Sub-Module (SM) and its gate drive circuit are

fitted on the battery modules so that, the power cables and the wires of gate signals are very short and introduce negligible parasitic inductance.

Figure 11 shows the response of the PLL system, under no load condition ($i_{abc}^* = 0$), when the damping ratio is set to

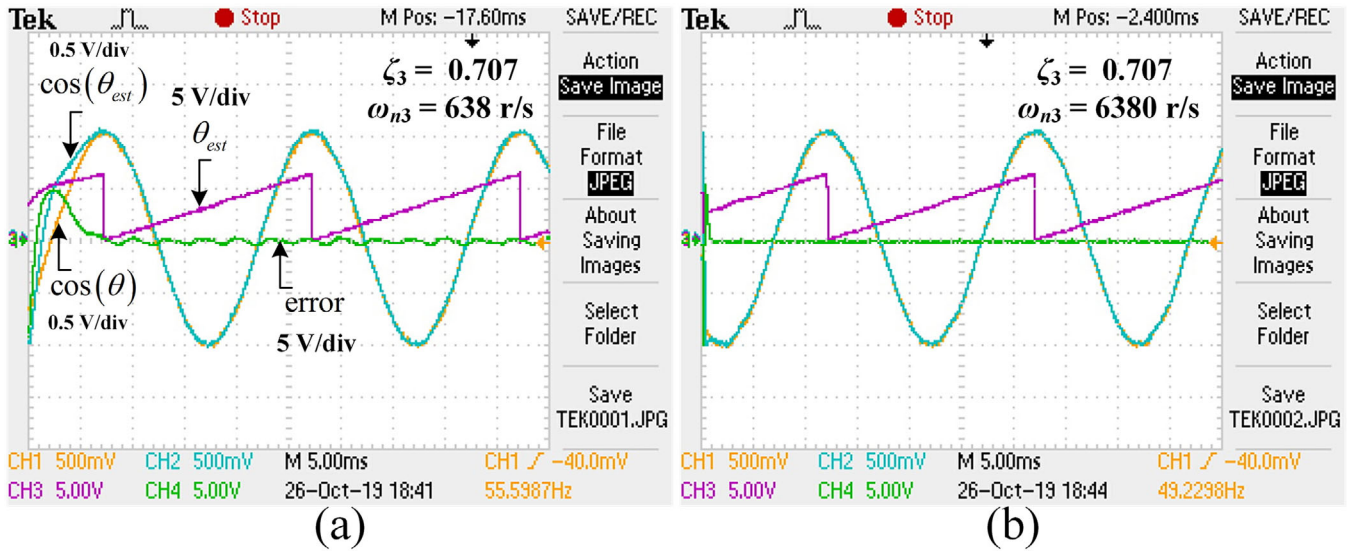


FIGURE 11 Experimental response of PLL (a) The responses of the PLL at natural frequency of 100 Hz. (b) The responses of the PLL at natural frequency of 1 kHz

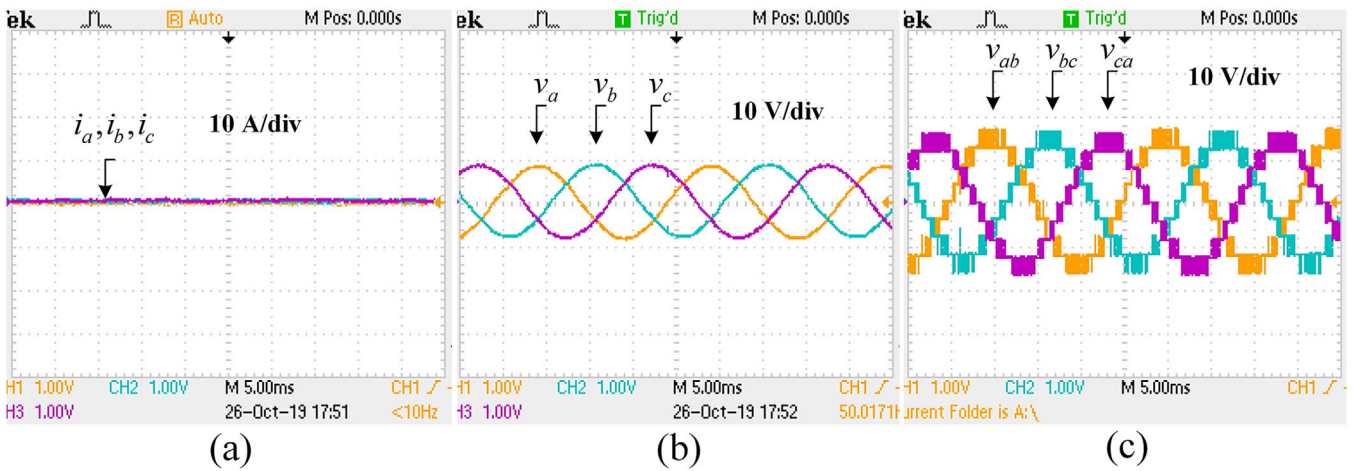


FIGURE 12 No load test. (a) The measured grid currents, (b) The measured grid voltages, (c) The converter line-to-line voltages

0.707 and the closed loop natural frequency is chosen equal to 100 Hz, and 1 kHz, respectively. The test confirms that the designed PLL work according to the simulations shown in Figure 7 with a faster dynamic response for a larger bandwidth of the controller. Figure 12 shows the converter line voltages and the grid phase voltages and currents. It is clear from the results that, the current controller is able to follow the reference grid current, and the grid current is almost zero. The line-to-line output voltage of the converter has five levels with a THD of 17.5% since the number of SMs within each arm is four.

In order to verify the response of the grid current controller, different peak values of i_{abc}^* have been applied, as shown in Figure 13. The vector i_{abc}^* has been set using Equation (11) to charge the cells via the DS-MMC at a unity power factor. The proposed controller shows a good capability of track-

ing the reference current. Figure 13 also shows the phase- a voltage at the secondary side of the transformer, the charging phase- a current with the corresponding reference current, the top and bottom arm voltages of phase- a , and the line-to-line voltage between the terminals a and b , all measured at p^* equal to 100, 200, and 300 W. It is clear from the results that, the current controller is able to track the reference grid current, and the grid current is almost sinusoidal for all the conditions shown in the figures and the proposed controller recharges the cells via the DS-MMC at unity power factor.

To test the SOC balancing algorithm, the initial SOC of the 24 Li-ion cells have been charged with an external DC supply at random levels to obtain an SOC unbalancing between the cells of around 15%. The cells have been charged at constant power of 345 W and the carrier frequency is set to

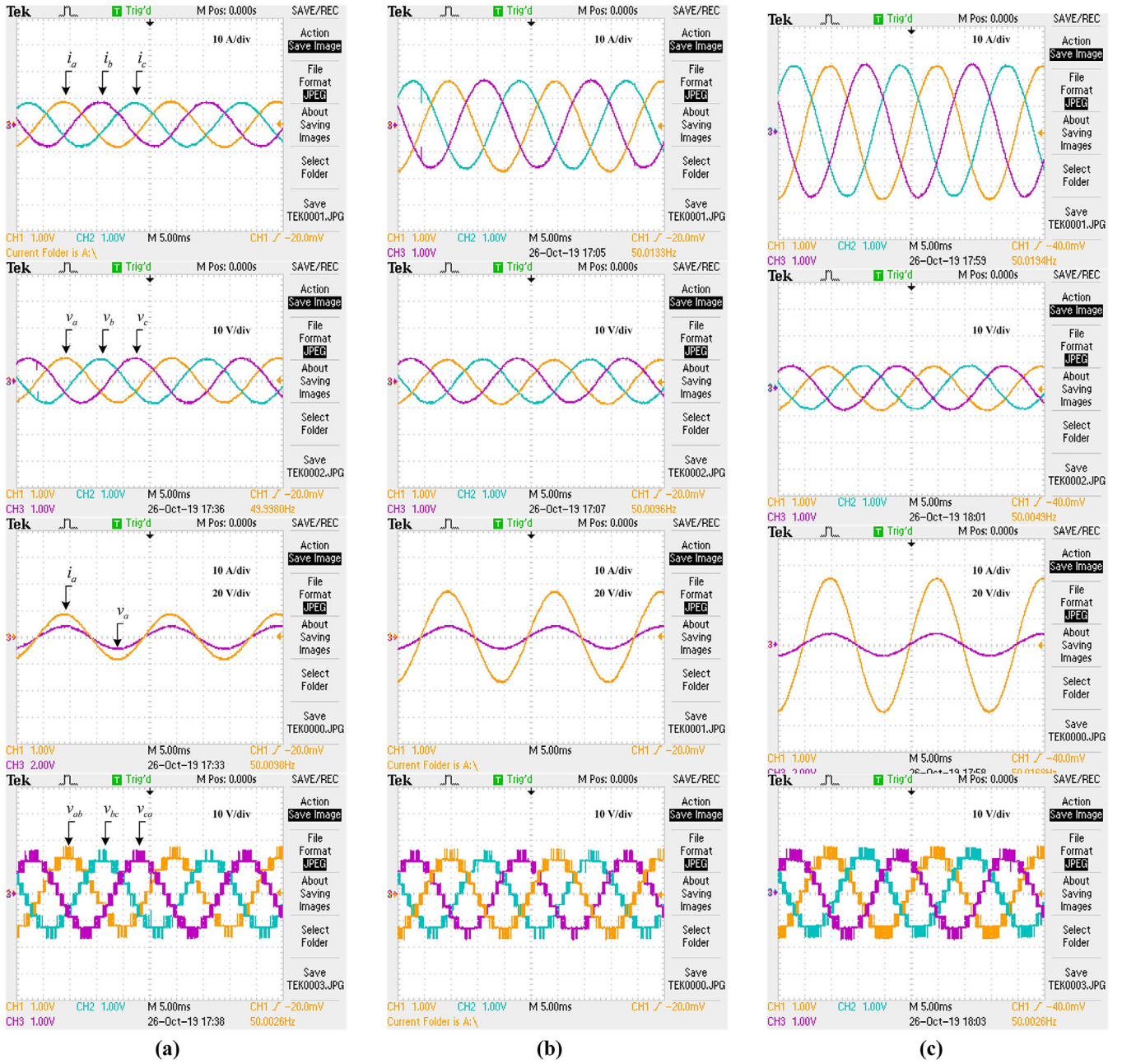


FIGURE 13 Experimental waveforms for a step change in p^* . (a) $p^* = 100$ W, (b) $p^* = 200$ W, (c) $p^* = 300$ W

2.25 kHz. Table 4 summarises the control gains used for the experiment.

Figure 14 shows that the balancing controller equalizes the SOC of all the battery cells towards the same level within the first 37 minutes of the recharge process. This is $1.7\times$ faster than a typical active balancing circuit [29], because the circulating current responsible for the balancing has the same value of the rated current of the DS-MCC. Figure 14 shows also the converter line-to-line voltages, the phase grid voltage at the output

of the transformer and the grid current, measured at $t = 200$ s and $t = 2,900$ s in order to demonstrate that they are not affected by the balancing control. The grid current is almost sinusoidal in both conditions without the need of any intermediate filter and the converter charges the cells at unity power factor. The reference currents do not follow exactly the grid currents because of the PLL errors caused by the grid phase unbalancing and harmonics. Figure 15 shows the simulated results under the same experiment conditions for comparison purposes.

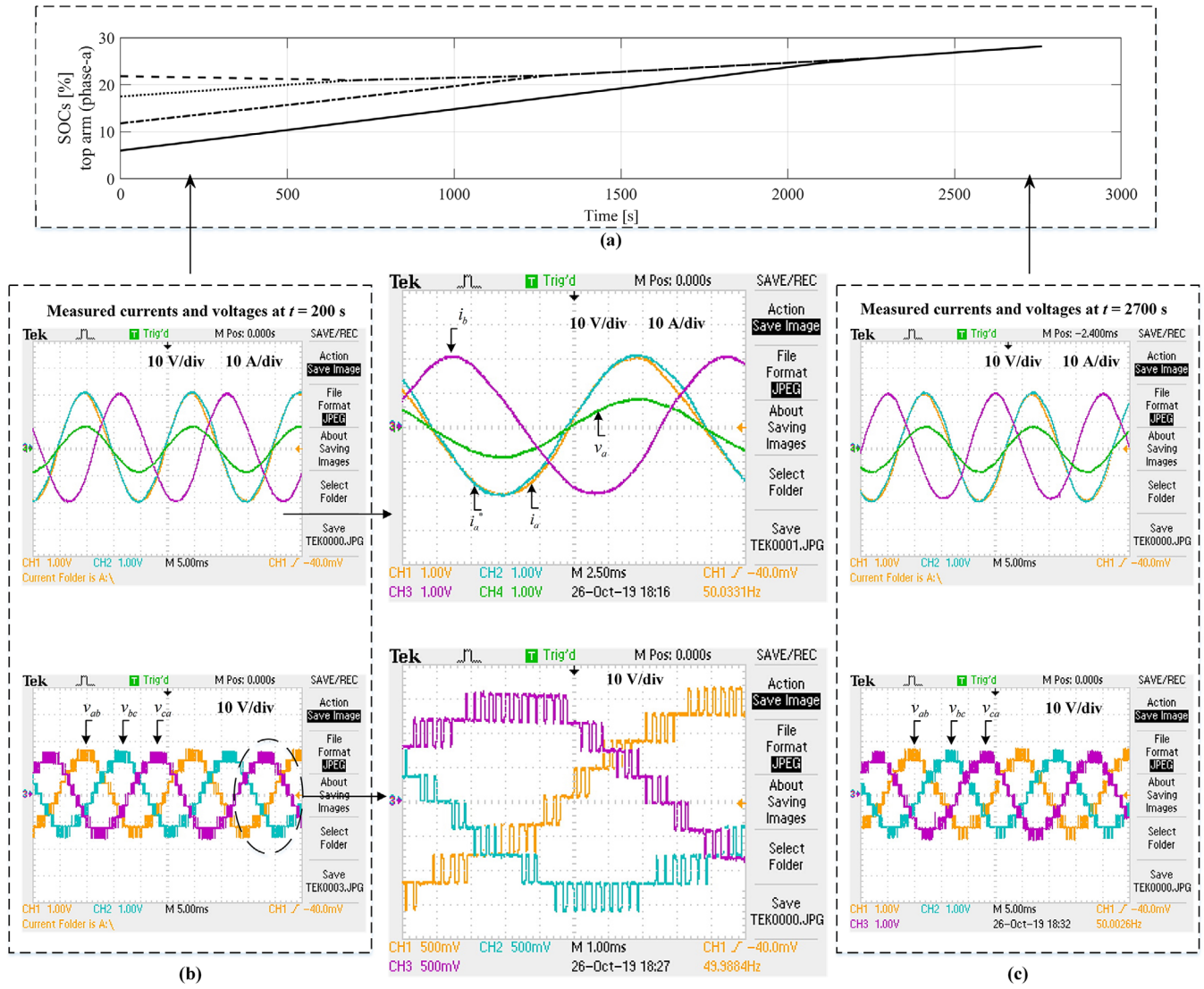


FIGURE 14 (Experimental results) (a) The SOCs, (b) The grid's phase- a voltage, grid's phase currents, and the converter's line-to-line voltages measured at $t = 200$ s, (c) The grid's phase- a voltage, grid's phase currents, and the converter's line-to-line voltages measured at $t = 2,700$ s

6 | COMPARISON WITH OTHER ACTIVE BALANCING TOPOLOGIES AND RELIABILITY ASSESSMENT

6.1 | Comparison with other active balancing circuits

One of the primary advantages of the proposed topology is to use the full load current to balance the Li-ion cells without the limitations of the low-power circuits of standard active balancing methods (5 A for the topology in [29]). The same converter is used to drive the traction motor or charge the cells from the grid at the same time of cell balancing. These characteristics lead to balancing the cells very quickly without extra energy losses in the auxiliary hardware required for conventional BMSs.

To highlight the capabilities of the proposed converter for the use with EVs, the authors have already compared it with the

most common active cell balancing methods (given in literature) in [31] and [32]. The comparison was in terms of size, cost, balancing time, and the hardware elements required as a function of the number of cells.

To verify the performance of the proposed converter, the balancing time has been compared with a new approach of active charge cell balancing (proposed in [29]). This method can balance the cells very quickly with acceptable energy losses. For the purpose of the comparison, the proposed converter has been tested with 8 Li-ion cells per each arm with a nominal capacity of 10 Ah. An average SOC of 50% and a standard deviation of 2% ($\sigma_0 = 2\%$) is assumed. The maximum charge imbalance decreases from 8% to standard deviation reaches $0.1\sigma_0$ within 400 s compared to 680 s necessary for the balancing method proposed in [29]. A comparison based on numerical simulations shows a reduction in balancing time by 58.82 % for randomly distributed cells. In the proposed converter, the balancing time

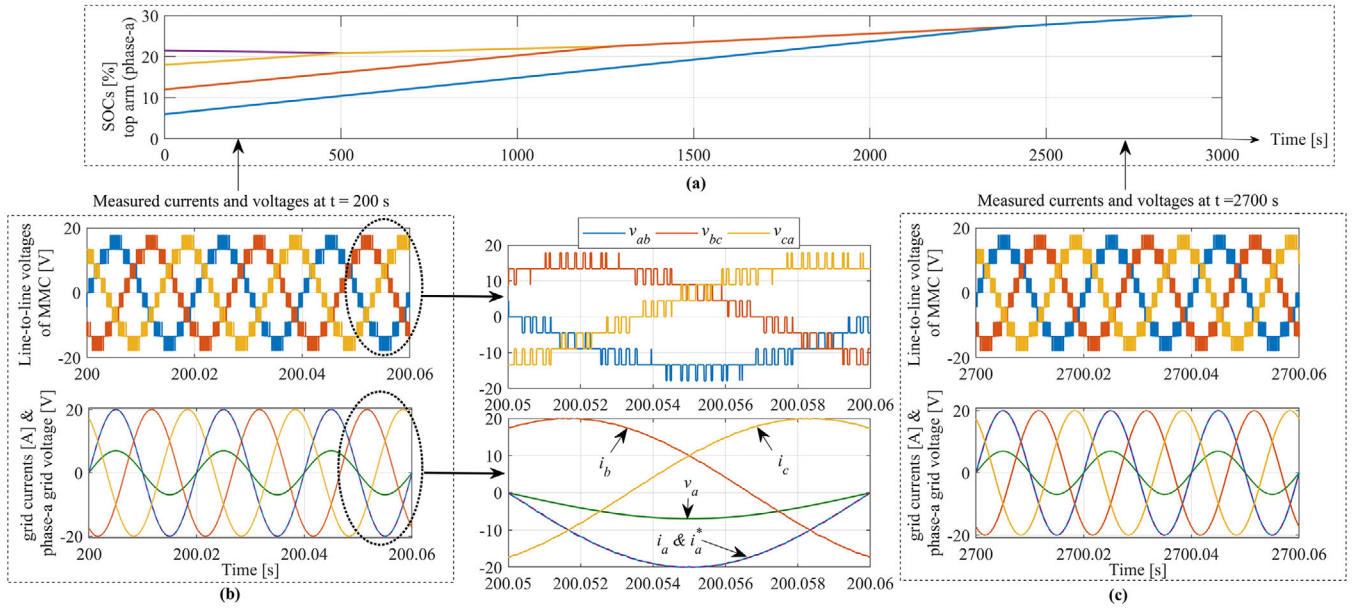


FIGURE 15 (Simulation results) (a) The SOCs, (b) The grid's phase-*a* voltage, grid's phase currents, and the converter's line-to-line voltages measured at $t = 200$ s, (c) The grid's phase-*a* voltage, grid's phase currents, and the converter's line-to-line voltages measured at $t = 2,700$ s

TABLE 4 Control gains of controllers used in experiment

Gain	Value	Control parameters
k_1	47.9831	$\zeta_1 = 35.355, \omega_{n1} = 0.0025 \text{ r/s}$
k_2	0.0017	
k_3	47.9831	$\zeta_2 = 35.355, \omega_{n2} = 0.0013 \text{ r/s}$
k_4	0.00085	
k_5	0.4443	$\tau = 112.5 \mu\text{s}$
k_6	-549.443	$\zeta_3 = 0.707, \omega_{n3} = 6380 \text{ r/s}$
k_7	-222.2	
k_8	1	$\zeta_4 = 7, \omega_{n4} = 1257 \text{ r/s}$
k_9	25	

can be further reduced since the converter can use the full load current to balance the cells, without the limitations of the low-power circuits of standard active balancing methods (5 A for the topology in [29]).

6.2 | Reliability assessment

Traditional two-level inverters consists of six power switches. Assuming that r_s is the static reliability of a single power switch, the reliability of the converter will be r_s^6 since all of the six switches are required to operate [33]. For the DS-MMC, the fault of a switch does not compromise the entire operation of the converter since the faulty module can be bypassed. Under fault condition in one of the SMs, the leg where the fault occurred will have m levels instead of $m + 1$ levels and the converter stays operational, but with a lower output voltage.

Therefore, the reliability of the converter depends on the power output required. Assuming that the motor rated power is P_r , then the range of the output power required is [31]:

$$\frac{\tilde{\zeta} - 1}{m} P_r \leq P \leq \frac{\tilde{\zeta}}{m} P_r, \quad (16)$$

where $\tilde{\zeta}$ is the number of healthy modules in the leg. The DS-MMC consists of two sets of star-configured converter arms (top and bottom arms) which are connected in parallel. Since each SM consists of two switches, the reliability of each SM is p^2 . Using the theory on partial redundancy and cumulative binomial distribution function, the reliability of the proposed modular multilevel converter, assuming equal reliabilities of both top and bottom arms, is given by:

$$R = R_t + R_b - R_t R_b; \quad R_t = R_b$$

$$R = 2 \left(\sum_{i=\tilde{\zeta}}^m \binom{m}{i} (r_s^2)^i (1 - r_s^2)^{m-i} \right)^3 - \left(\sum_{i=\tilde{\zeta}}^m \binom{m}{i} (r_s^2)^i (1 - r_s^2)^{m-i} \right)^6 \quad (17)$$

On the other hand, the CHB converter consists of only one set of star-configured converter legs. The reliability of each SM/leg is p^4 since each SM consists of four switches. Therefore, the static reliability of the CHB converter can be calculated as:

$$R = \left(\sum_{i=\tilde{\zeta}}^m \binom{m}{i} (r_s^4)^i (1 - r_s^4)^{m-i} \right)^3, \quad (18)$$

The reliabilities of two-level inverter and CHB have been compared with the reliability of the DS-MMC topology, assuming $m = 84$ and $r_s = 0.9$. The reliability of the DS-MMC is higher than the reliability of the traditional inverter for a wider range of power. However, the reliability decreases when the full load power is required since all SMs must be bypassed or inserted in the leg all the time to produce the rated voltage. The DS-MMC superiors up to a power of 0.8 pu, whereas CHB is superior up to power of 0.62 pu. The reliability of the two-level inverters is highly affected by the value of r_s . On the other hand, the reliability of proposed topology is always constant regardless of the value of r_s for a large range of the output power. It should be mentioned that the comparison does not consider the reliability of cell balancing circuit used for the traditional inverter, so the DS-MMC is penalised.

7 | DISADVANTAGES AND POSSIBLE SOLUTIONS

7.1 | Cost and size

In this new topology, the battery cells are connected in series via the switch SMs to individually discharge and recharge each cell where each switch SM is constructed from a half bridge converter. The proposed topology does not use high-voltage switches, which occupy large area and, therefore, the cost and size are significantly reduced. In the hardware design, each SM and its gate drive circuit have been fitted on the battery modules so that, the power cables and the wires of gate signals are very short and light. In addition, there is no need of balancing circuits, that require hundreds of semiconductor devices (albeit with low power) but the same degree of complexity in terms of gate drivers. Thus, the converter has small balancing time with acceptable size and cost.

7.2 | Complexity of controllability

The traditional active balancing circuits have large number of high current switches, typically 1–4 switches/cell. On the other hand, the proposed converter (Type 2) has two low-voltage high-current switches/cell. However, these switches have the same type of gate driver control; therefore, the controllability of the proposed circuit has the same degree of complexity of most common active balancing circuits. Nevertheless, modern controllers such as Field Programmable Gate Array (FPGA) can handle a large number of digital output signals to run the switches and execute the SOC balancing algorithm for all the cells used in the proposed converter.

7.3 | Efficiency

One of the main drawbacks of the proposed topology is the increased conduction losses, if compared with traditional inverters due to the high number of devices conducting in series. This

can be mitigated by the lower switching losses, by an appropriate choice of the semiconductor devices, and by a proper selection of modulation strategy.

The efficiency assessment of the converter for BEVs has been introduced by the authors in [32]. Using a proper selection of modulation strategy, the switching losses of the DS-MMC are much lower than those of traditional inverters and the global efficiency is comparable and even higher in some cases. It should be mentioned that, the comparison in [32] does not consider the power losses in the cell balancing converter used for the traditional inverter, so the DS-MMC is penalised.

7.4 | Buffer inductors

One of the disadvantages of DS-MMC is the use of buffer inductors between the converter arms to limit the circulating current. Each two buffer inductors/leg can be replaced with a single coupled buffer inductor for a size reduction in the magnetic components. The use of the coupled inductor results in bringing considerable reductions in size, weight, and cost to the magnetic core [40].

7.5 | Common mode voltage and leakage currents

The output voltage waveform produced by the conventional two-level inverter is a series of square wave pulses. The pulses have voltage spikes of large magnitudes with high slew rate (high dv/dt), which can lead to damage and premature failure of the motor winding insulation [41].

Another drawback of driving traction motors with two-level inverters is, generation of a voltage between the neutral point and the iron core of the motor, called as common mode voltage (CMV) due to the instantaneous imbalance of three phase voltages. The magnitude of the CMV spikes increases with the switching frequency. The high amplitude of CMV and its high dv/dt increase the motor shaft voltage, resulting in excessive bearing currents when the shaft voltage exceeds the breakdown voltage of the bearing grease [41].

The proposed converter can reduce the CMV since the output AC voltage produced by the converter is stepped in smaller increments (lower dv/dt) and the converter is able to operate at a lower switching frequency with good quality of output voltage. The CMV can be further reduced in the proposed converter by applying proper modulation technique such as Space Vector Modulation (SVM), Phase Opposition Disposition Pulse Width Modulation (POD-PWM) techniques etc... [42, 43].

8 | CONCLUSION

This paper proposes a new battery charger for electric vehicles based on modular multilevel converters. The converter produces an extremely low distortion of the output voltage, with direct benefits for the operations as a battery charger. For this

reason, the grid filter can be eliminated with benefits on the hardware costs. The proposed charger integrates the BMS in the power converter control and eliminates the need for additional balancing circuits. The state of charges of all battery cells are managed by SOC balancing controllers without affecting the grid voltage and current. The battery cells are charged from the utility grid and the charging operation is controlled via a proportional resonant current controller with a phase-locked loop to charge the cells at unity power factor.

The proposed vehicle's battery charger has been validated with computer simulations in Matlab/Simulink and experiments on a converter prototype with four sub-modules per arm, having line voltage of 10 V and line current of 50 A. The tests have demonstrated the negligible distortion of the grid current and the correct operations of the battery charger. The proposed charger enables a new concept of charging battery cells which are directly embedded in the power converter and is the recommended topology to eliminate balancing circuits and increase the balancing speed of the battery cells by a factor of 170%. Therefore, this converter is the most favourable for fast and ultra-fast charging of batteries, where differences in the state-of-charge are the main limiting factors of the charging speed.

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