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Design and Model of Series Connected High Voltage DC Multipliers

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***Abstract*- Generation of high DC voltages is necessary for feeding many technical applications and testing the insulation material of high voltage DC transmission lines and AC power cables with long lengths. The paper proposes a modular multiplier high voltage DC generator with integrated Cockcroft-Walton (CW) circuits. In this new topology, Cockcroft-Walton circuits are connected in series to produce a high DC output voltage with low regulation factor (< 2 %) and a negligible ripple factor without the need for costly filters to produce a nearly constant output voltage. The modules are fed by low input AC voltage sources that have the same magnitude and frequency. Numerical simulations using MATLAB/Simulink confirm the viability of the proposed generator. The generator is finally validated by experimental tests on a kV-size prototype.**

***Index Terms*—Cockcroft-Walton circuit, multiplier, ripple factor, regulation, harmonics**.

I. Introduction

Generation of high DC voltages serve as test voltages for elements of high voltage DC transmission lines and long AC power cables. Normally, in high voltage testing, the current under conditions of failure is limited to a small value (less than an ampere in the case of DC). High DC voltage is also necessary to feed many technical applications, such as communication electronics, X-ray equipment, electron microscopes, capacitor chargers, electrostatic precipitators, paint spraying devices and surface coating devices. Impulse generator charging units also require high DC voltages of about 100 to 200 kV and output currents of about 100 mA. The charging generator should have a ripple of very small magnitude without the use of costly filters to smoothen the ripple [1]-[3].

The generation of high DC voltages are usually obtained from AC voltages by rectification process to produce a high ratio of DC output to AC input voltage. Direct voltages are often superimposed by periodic functions. Therefore, IEC 60060-1 defines the arithmetic mean value as the DC test voltage and the ripple of the output waveform is described by the ripple factor, which should not be more than 3% for DC voltage tests [4], [5].

The simplest circuit for generation of high DC voltage is the half wave rectifier. The AC voltage source, which is normally available in high voltage laboratories is supplemented with a rectifier and a smoothing capacitor to form the half-wave rectifier circuit. The half wave rectifiers produce DC voltages less than the maximum value of the AC supply voltage. The size of the circuit becomes very large if a high and a pure DC output voltage is required. The high voltage transformer may also get saturated if the amplitude of direct current is comparable with the nominal alternating current of the transformer [6]. High-voltage half-wave rectifiers always consist of a series connection of several semiconductor diodes whose reverse voltage is restricted to a few kV. This is a problem for potential distribution in the reverse blocking state, since an unequal voltage distribution would lead to overstress and destruction of individual diodes [5].

When higher DC voltages are required to be generated, voltage doubler circuits are used. These circuits are able to produce an average output voltage twice the maximum value of the AC supply voltage. However, they have many disadvantages such as poor voltage regulation, high capacitor voltage ratings, and high ripples, and harmonics in the output voltage.

Cascaded voltage doublers are used when larger output voltages are needed without changing the input transformer voltage level. The circuits are able to produce voltage more than twice the peak value of input voltage. The cascade doubler circuit has major feature than other types since it has higher power capabilities. However, the cascading of every stage would thus require an additional isolating transformer which makes this circuit less economical for high number of stages [7].

Cascaded voltage doubler circuits for higher voltages are cumbersome and require too many supplies and isolating transformers. It is possible to generate very high DC voltages from single supply transformers by extending the simple voltage doubler circuits using the Cockcroft-Walton principle. This is simple and compact when the load current requirement is less than one milliampere. The main advantage of the Cockcroft-Walton circuit is to generate high voltage DC from power supply without need an expensive high voltage transformer, therefore the cost and size of the circuit is small. Moreover, it is simple in implementation since it consists of cascaded connection of diodes and capacitors. On the other hand, this topology has many disadvantages such as high regulation and ripple factors for large number of stages [8]-[10].

One of the problems with the traditional Cockroft-Walton High Voltage Direct Current (HVDC) multiplier circuit is the voltage drop, which is proportional to the cube of the number of stages. Therefore, a high effective number of stages

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produces undesirable high voltage loss along the generator, which limits the power supplied by the generator.

Another problem is the peak-to-peak ripple voltage, which is proportional to the square of the number of stages. As the number of stages increases, the capacitance of the circuit must be increased to reduce the ripple as well as to keep the overall voltage drop low. However, the use of large capacitors means that the total energy stored in the circuit is high. For many high voltage applications, very fast high voltage breakdown is likely to occur in the load, a large amount of stored energy causes sparks with attendant substantial damage.

The main contribution of this paper is to model, simulate and design a series connected high voltage multiplier using a relatively simple circuit configuration with embedded multiplier circuits, which can be readily designed. The proposed generator is able to provide a simpler solution to the problems that arise in the Cockroft-Walton topology and in the alternative rectifier circuits suggested by those in the art. It is able to produce a high DC output voltage (an adequate voltage output) with low regulation factor and a negligible ripple factor without the need for costly filters to produce a nearly constant output voltage. The voltage drop along the circuit is relatively low and provides for better voltage regulation than do conventional multiplier circuits.

As a second advantage for the proposed generator, a reduction of capacitor size and cost is possible if the proposed generator is constructed to produce the same voltage drop of the traditional Cockroft-Walton circuit. The use of smaller capacitors in such generators reduces the extractable stored energy. Accordingly, less damage will occur to the load in the case of a fast breakdown. Moreover, the generator has a relatively short response time in comparison with the standard CW circuits and therefore, relatively it is easy to regulate it.

In summary, the use of such modular multiplier HVDC generator, together with isolated transformers substantially reduces the voltage drop and ripple or, conversely, allows for the use of smaller capacitors, thereby reducing the stored energy, in comparison with the standard CW circuits.

Mathematical models for ripple factor, regulation, and harmonic contents of the output DC voltage have been presented in the paper (section II), and verified by numerical simulation and experiment (sections III & IV).

This paper is organised in four sections and the rest of the paper is organised as follows: section II introduces the configuration and the basic principle of operation of the proposed generator. The section also introduces the mathematical model of calculating the ripple and regulation factors for the proposed generator. Section III presents the simulation results for the sample case of the HVDC generator and the comparison between the proposed and the traditional Cockroft-Walton generators; section V validates with experimental results the proposed generator.

II. Modular Multiplier Conversion System

The layout of the proposed conversion system is shown in the schematic of Fig. 1. The generator consists of m cascaded sub-modules (SMs)), where each SM consists of a Cockcroft-Walton (CW) circuit with n stages with a floating AC source. The generator is fed by two ways, as shown in Fig. 2:

- Method 1: Low power multiphase synchronous machine with star-connected stator windings. In this method, the modules are supplied by m isolated sources that have the same magnitude, frequency and shifted from each other by an angle of $2\pi/m$.
- Method 2: Low power single-phase AC source. In this method, the modules are supplied via multi-winding transformer (m secondary windings) that have the same magnitude, frequency and phase.

Assuming that each source voltage has a peak value of V, the voltage of the k-th phase, $v_{s,k}$, is given by:

$$v_{s,k} = V\sin\left(\omega t + \varphi_k\right);\quad k \in \left\{1 \quad 2 \quad \cdots \quad m\right\}; \tag{1}$$

where ω is the electric radian frequency of the source and φ_k is the phase angle of the source, which is $2\pi\,(k-1)/m$ for method 1 and constant for method 2. Fig. 2 shows the possible methods of feeding the proposed generator.

A. Operating Principle of the Proposed Generator

The operation principle of the Cockcroft-Walton circuit can be explained with reference again to Fig. 1. The capacitor, C_1, is charged through diode, D_1 to a voltage of V during the negative half cycle. When the source voltage rises to positive V during the next half cycle, the capacitor, C_2, is charged through diode, D_2 to a voltage of $2V$. The voltage at node 1 of module k, with respect to 0 potential node, is given by:

$$v_{10,k} = V + v_{s,k} = V + V\sin\left(\omega t + \varphi_k\right). \tag{2}$$

When $v_{10,k}$ is zero, the capacitor C_3 is charged to the potential $2V$ through diode, D_3. The next voltage variation of $v_{10,k}$ from zero to $2V$ will force the diode, D_4, to conduct, so that also C_4 will be charged to a voltage of $2V$.

The steady state voltages at nodes 1, 3 … $2n-1$, with respect to 0 potential, are given by:

$$v_{z0,k} = zV + V\sin\left(\omega t + \varphi_k\right);\quad z \in \left\{1 \quad 3 \quad \cdots \quad 2n-1\right\} \tag{3}$$

while the steady state voltages at nodes 2, 4 … $2n$, with respect to 0 potential, are given by:

$$v_{h0,k} = hV;\quad h \in \left\{2 \quad 4 \quad \cdots \quad 2n\right\} \tag{4}$$

Therefore, the high voltage output of k-th SM, $v_{o,k}$, will reach a maximum voltage of $2nV$ when $h = 2n$, and the maximum value of the total output voltage, v_o, of the cascaded m SMs is given by:

$$v_o = \sum_{k=1}^{m} v_{o,k} = \sum_{k=1}^{m} 2nV = 2mnV \tag{5}$$

B. Ripple and Regulation Factors

Fig. 3 shows the typical waveform of the output voltage of each SM in the proposed converter and its harmonic spectrum. It is clear that, the output voltage of each SM will never reach the value of $2nV$ and there will also be a ripple on the voltage. The ripple factor of the output voltage, RF, can be calculated as:

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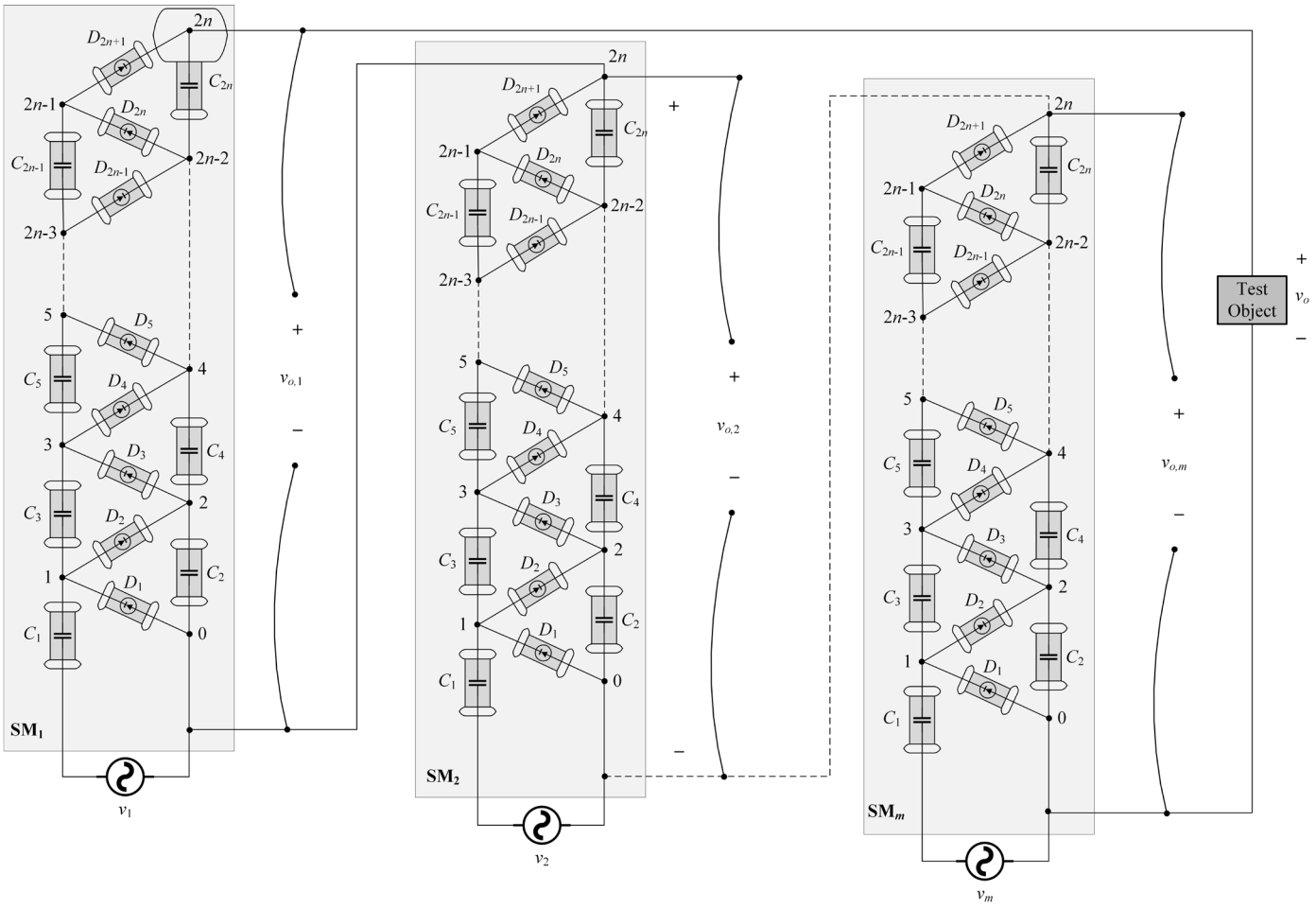

Fig. 1. Layout of the proposed modular high voltage DC generator with embedded Cockcroft-Walton circuits.

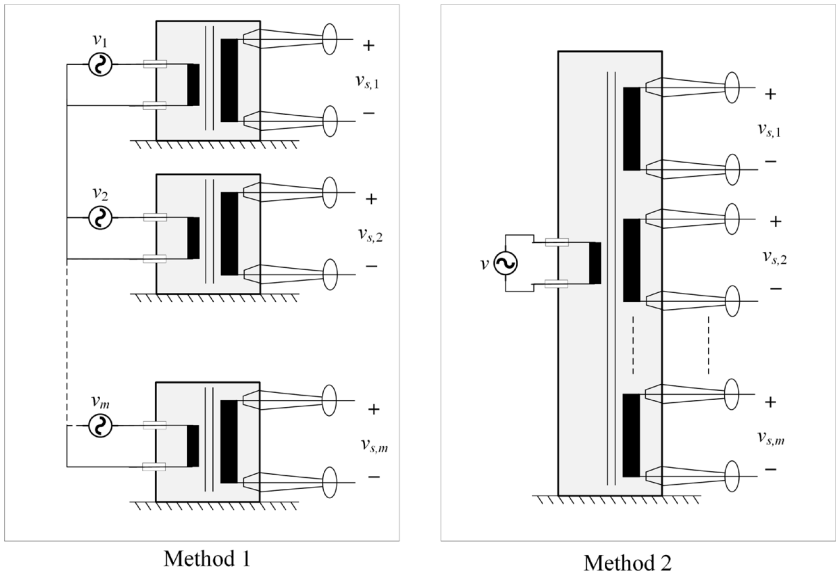

Fig. 2. Methods of feeding the proposed generator.

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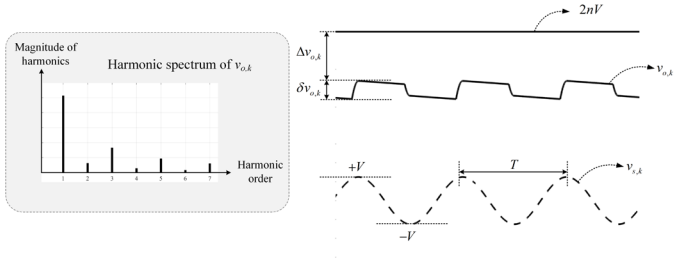

Fig. 3. The typical steady state output voltage waveform of each SM and its frequency spectrum.

$$RF = \frac{\sqrt{\sum_{h=1}^{\infty} V_h^{\,2}}}{v_{o,k,\mathrm{avg}}} \tag{6}$$

where V_h is the RMS voltage of the h-th harmonic and $v_{o,k,avg}$ is the mean value of the output voltage. On the other hand, the regulation factor of the output voltage, R, is calculated as:

$$R = \frac{\Delta v_{o,k}}{2nV} \tag{7}$$

It is clear that the waveform contains a significant odd harmonics and insignificant even harmonics. The odd harmonics are associated with the half-wave symmetrical shape of the signal.

Suppose that a charge q is transferred to the load per each cycle of period T. This charge comes from capacitors C_2, C_4 … C_{2n}, and is given by:

$$q = \int_0^T I\,dt = IT = \frac{I}{f} \tag{8}$$

where f is the frequency of the source and I is the load current.

The capacitors C_2, C_4 … C_{2n}, are charged during the positive half cycle of the sources while the capacitors C_1, C_3 … C_{2n-1}, are charged in the next half cycle (transfer half cycle). Refer to Fig. 1, assuming that the voltage at node $2n$ is $2nV$. This voltage will be discharged through the load resistance and must be regained during the charging cycle for stable operation of the generator. The capacitor C_{2n} is therefore supplied a charge q from C_{2n-1} and, therefore the peak-to-peak ripple at C_{2n} is q/C_{2n}. The capacitor C_{2n-2} must acquire a charge of $2q$ so that it can supply q charge to the load and q charge to C_{2n-1}. Therefore, the peak-to-peak ripple at C_{2n-2} is $2q/C_{2n-2}$. Similarly, the capacitor C_{2n-4} must acquire for a charge $3q$ so that it can supply a charge q to the load and $2q$ charge to the capacitor C_{2n-3} in the next half cycle (transfer half cycle). Therefore, the peak-to-peak ripple at C_{2n-4} is $3q/C_{2n-4}$. Finally, the capacitor C_2 must acquire for a charge nq so that it can supply a charge q to the load and $(n-1)q$ charge to the capacitor C_3 in the next half cycle (transfer half cycle). Therefore, the peak-to-peak ripple at C_2 is nq/C_2.

Assuming that $r(t)$ is the normalized ripple signal with a peak to peak value of 1 pu, then the ripple function of k-th SM, $\delta v_{o,k}$, which is the sum of all ripples at capacitors C_2, C_4 … C_{2n}, within that SM, can be expressed as:

$$\delta v_{o,k} = \left(\sum_{i=1}^{n} \frac{q}{C_{2n-2i+2}} i\right) r\left(t - \varphi_k/\omega\right) \tag{9}$$

Assuming that all capacitances be equal to C, then the ripple at k-th SM can be further represented by:

$$\begin{aligned} \delta v_{o,k} &= \left[\sum_{i=1}^{n} \frac{q}{C} i\right] r\left(t - \varphi_k/\omega\right) = \left[\frac{q}{C}\sum_{i=1}^{n} i\right] r\left(t - \varphi_k/\omega\right) \\ &= \left[\frac{q}{2C} n\left(n+1\right)\right] r\left(t - \varphi_k/\omega\right) \end{aligned} \tag{10}$$

and the total ripple at the output of the proposed generator is given by:

$$\delta v_o = \sum_{k=1}^{m} \delta v_{o,k} = \left[\frac{q}{2C} n\left(n+1\right)\right] \sum_{k=1}^{m} r\left(t - \varphi_k/\omega\right) \tag{11}$$

while the ripple at the output of the traditional CW generator is given by [1]-[3]:

$$\delta v_{o,CW} = \frac{q}{2C} N\left(N+1\right) r\left(t\right) \tag{12}$$

where N is the number of stages. Assuming that both generators have the same number of elements, then N will be given by:

$$N = mn \tag{13}$$

If the SMs are supplied using method 1, then the peak-to-peak ripple at the output of the proposed generator, δV_o, goes to zero as m increases to large value:

$$\delta V_o = \lim_{m\to\infty} \delta v_o = \left[\frac{q}{2C} n\left(n+1\right)\right] \lim_{m\to\infty} \sum_{k=1}^{m} r\left(t - \varphi_k/\omega\right) = 0 \tag{14}$$

On the other hand, if the SMs are supplied using method 2, then φ_k is constant for all k. In this case, the peak-to-peak ripple at the output of the proposed generator will be smaller than that in the traditional CW generator:

$$\begin{aligned} &\delta V_o = \frac{q}{2C} mn\left(n+1\right) \qquad \delta V_{o,CW} = \frac{q}{2C} N\left(N+1\right) \\ &\delta V_o < \delta V_{o,CW} \ \text{ since } \ mn\left(n+1\right) < N\left(N+1\right) \end{aligned} \tag{15}$$

Equation (15) shows the proposed generator has lower RF in comparisons with the traditional CW generator even all SMs are supplied by isolated AC sources that have the same magnitude, frequency, and phase.

Assuming that the diodes are ideal and there is no voltage drop within the AC sources, the capacitor C_1 will be charged up to the full voltage V during the negative half cycle. Since the capacitor, C_2, has lost a total charge of nq during the previous cycle and C_1 has to replace this lost charge, C_2 in all SMs will be charged to a voltage given by:

$$v_{C_2,\max} = 2V - n\frac{q}{C_1} \tag{16}$$

When the source voltage reaches $-V$, the capacitor C_2 will transfer equal amounts of q to C_3, C_5 … C_{2n-1} and the load during the period T. Therefore, C_3 will be charged up to a maximum voltage given by:

$$v_{C_3,\max} = v_{C_2,\max} - n\frac{q}{C_2} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2} \tag{17}$$

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Since the capacitor C_4 has lost a total charge of $(n-1)q$ during the previous cycle and C_3 has to replace this lost charge, C_4 will be charged to a voltage given by:

$$v_{C_4,\max} = v_{C_3,\max} - (n-1)\frac{q}{C_3} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3} \quad (18)$$

When the source voltage reaches $-V$, the capacitor C_4 will transfer equal amounts of q to C_5, C_7 … C_{2n-1} and the load during the period T. Therefore, C_5 will be charged up to a maximum voltage given by:

$$\begin{aligned} v_{C_5,\max} &= v_{C_4,\max} - (n-1)\frac{q}{C_4} \\ &= 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3} - (n-1)\frac{q}{C_4} \end{aligned} \quad (19)$$

Since the capacitor C_6 has lost a total charge of $(n-2)q$ during the previous cycle and C_5 has to replace this lost charge, C_6 will be charged to a voltage given by:

$$\begin{aligned} v_{C_6,\max} &= v_{C_5,\max} - (n-2)\frac{q}{C_5} \\ &= 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3} - (n-1)\frac{q}{C_4} - (n-2)\frac{q}{C_5} \end{aligned} \quad (20)$$

If all the capacitors within all SMs are equal and be equal to C, the voltage drop across capacitors C_2, C_4 … C_{2n}, within each SM, can be expressed as:

$$\begin{aligned} \Delta v_{C_{2,k}} &= \frac{q}{C}[n] \\ \Delta v_{C_{4,k}} &= \frac{q}{C}[2n + (n-1)] \\ \Delta v_{C_{6,k}} &= \frac{q}{C}[2n + 2(n-1) + (n-2)] \\ &\vdots \\ \Delta v_{C_{2n,k}} &= \frac{q}{C}[2n + 2(n-1) + 2(n-2) + \cdots + 2\times 2 + 1] \end{aligned} \quad (21)$$

where C is the generator capacitance. Consequently, the total voltage drop across one SM, can be expressed as:

$$\Delta v_{o,k} = \sum_{i=2,4,\cdots}^{n} \Delta v_{C_{i,k}} = \frac{q}{C}\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{1}{6}n\right] \quad (22)$$

and the total voltage drop across all cascaded SMs, can be expressed as:

$$\begin{aligned} \Delta v_o &= \sum_{k=1,2,\cdots}^{m} \Delta v_{o,k} = \frac{q}{C} m\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{1}{6}n\right] \\ &= \frac{q}{C}\left[\frac{2}{3}\frac{N^3}{m^2} + \frac{1}{2}\frac{N^2}{m} - \frac{1}{6}N\right] \end{aligned} \quad (23)$$

while the total voltage drop across the N stages of the traditional CW generator is given by [1]-[3]:

$$\Delta v_{o,\mathrm{CW}} = \frac{q}{C}\left[\frac{2}{3}N^3 + \frac{1}{2}N^2 - \frac{1}{6}N\right] > \Delta v_o \quad (24)$$

Using (23) and (24), the relation between the voltage loss along the proposed generator and the voltage drop across the traditional CW circuit is given by:

$$\frac{\Delta v_o}{\Delta v_{o,\mathrm{CW}}} = \frac{R}{R_{\mathrm{CW}}} = \frac{4(N^3/m^2) + 3(N^2/m) - N}{4N^3 + 3N^2 - N} \quad (25)$$

where R and R_{CW} are the regulation factors of the proposed generator and the traditional CW circuit, respectively.

For a Cockroft-Walton generator with N = 12 stages, the proposed circuit is able to produce a high DC output voltage with lower regulation factor by choosing m = 6 and n = 2 (i.e. $R = 0.034R_{\mathrm{CW}}$), which means the regulation factor is reduced by factor of 96.4 %.

For a given number of stages and modules, the voltage drop at the output of the proposed generator is small, in comparison with the traditional CW generator. Therefore, the use of this generator eliminates the need for high supply frequencies and regulation systems to control the AC supply voltage, which are necessary if a stable and constant output voltage is required with fast response. However, the voltage drop at the output of the proposed generator will decrease inversely with the capacitance of the generator for a given number of elements at constant frequency and load current. Therefore, small values of generator capacitance can be used to produce the same voltage drop of CW circuit. Consequently, the generator has lower energy losses with acceptable size and cost in comparisons with the traditional CW generator.

The new value of the capacitance, C', can be obtained by equating the total voltage drop across all cascaded SMs of the proposed generator with the total voltage drop across the N stages of the traditional CW generator, assuming that both generators have the same number of elements ($N = mn$):

$$\begin{aligned} &\Delta v_o = \Delta v_{o,\mathrm{CW}} \\ &\frac{q}{C'}\left[\frac{2}{3}\frac{N^3}{m^2} + \frac{1}{2}\frac{N^2}{m} - \frac{1}{6}N\right] = \frac{q}{C}\left[\frac{2}{3}N^3 + \frac{1}{2}N^2 - \frac{1}{6}N\right] \\ &C' = C\left[\frac{4(N^3/m^2) + 3(N^2/m) - N}{4N^3 + 3N^2 - N}\right] << C \end{aligned} \quad (26)$$

With m SMs, the proposed generator can produce $2mnV$ DC voltage under no load condition. However, when it is loaded, the maximum output voltage is given by:

$$v_{o,\max} = 2mnV - \frac{q}{C} m\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{1}{6}n\right] \quad (27)$$

and the mean value of the output voltage is given by:

$$\begin{aligned} v_{o,avg} &\approx v_{o,\max} - \frac{\delta v_o}{2} \\ &= 2mnV - \frac{q}{C} m\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{1}{6}n\right] - \frac{1}{2}\delta V_o \end{aligned} \quad (28)$$

C. Harmonic Analysis

The instantaneous output voltage produced by the traditional CW circuit and its harmonics can be represented, using Fourier series, as:

$$v_o = f_0(N) + \sum_{h=1}^{\infty} V_{h,N} \sin\left(h(\omega t + \gamma)\right); \quad (29)$$

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where f_0 (N) is the mean value of the output voltage, $V_{h,N}$ is the magnitude of h-th harmonic of N stages generator, and γ is the phase angle of the main component. On the other hand, the instantaneous output voltage produced by each SM in the proposed generator can be represented, using Fourier series, as:

$$\begin{aligned} v_{o,k} &= f_0(n) + \sum_{h=1}^{\infty} V_{h,n} \sin\left(h\left(\omega t + \gamma_k\right)\right); \\ \gamma_k &= \gamma_1 + \frac{2\pi}{m}(k-1) \end{aligned} \tag{30}$$

where $f_0(n)$ is the mean value of the output voltage of k-th SM, $V_{h,n}$ is the magnitude of h-th harmonic of n stages SM which is less than $V_{h,n}$ since $n < N$, and γ_k is the phase angle of the main component of SM k. In this case, the instantaneous total output voltage produced by the generator is given by [11]:

$$\begin{aligned} v_o &= \sum_{k=1}^{m} v_{o,k} = v_{o,avg} + \sum_{k=1}^{m}\sum_{h=1}^{\infty} V_h \sin\left(h\left(\omega t + \gamma_k\right)\right) \\ &= v_{o,avg} + \sum_{h=1}^{\infty}\sum_{k=0}^{m-1} V_h \sin\left(h\left(\omega t + \gamma_1 + 2\pi k/m\right)\right) \\ &= v_{o,avg} + \sum_{h=1}^{\infty} B_h V_h \cos\left(h\left(\omega t + \gamma_1\right)\right); \\ B_h &= \frac{\sin\left((m-1)\pi h/m\right)\sin\left(\pi h\right)}{\sin\left(\pi h/m\right)} = 0; \quad h \neq m, 2m, 3m, \cdots \end{aligned} \tag{31}$$

Equation (31) shows that only the coefficients of the cosine series in the Fourier analysis are finite; those for the sine series are zero. The harmonics in the waveform of the generator output voltage appear at mf and its multiples, that is, at frequencies mf, $2mf$, $3mf$, and so on. Choosing m as an even integer results in an even symmetry. Therefore, only even harmonics are present and the odd harmonics disappear from the waveform of the output voltage.

If the SMs are supplied using method 2, then φ_k is constant for all k. In this case, the instantaneous total output voltage produced by the generator is given by:

$$\begin{aligned} v_o &= \sum_{k=1}^{m} v_{o,k} = v_{o,avg} + \sum_{k=1}^{m}\sum_{h=1}^{\infty} V_{h,n} \sin\left(h\left(\omega t + \gamma_1\right)\right) \\ &= v_{o,avg} + \sum_{h=1}^{\infty} m V_{h,n} \sin\left(h\left(\omega t + \gamma_1\right)\right) \end{aligned} \tag{32}$$

Equation (32) shows that, the generator has lower RF in comparisons with the traditional CW generator even all SMs are supplied by isolated AC sources that have the same magnitude and phase.

D. Voltage drop and power losses contributed by transformers

In the conventional Cockroft-Walton voltage multiplier, the input stage consists of a single-phase AC source that feeds a high voltage isolation transformer with rated apparent power of $S_{r,\mathrm{CW}}$. Neglecting the excitation branch in the equivalent circuit of the transformer, the transformer's apparent power can be expressed as:

$$S_{r,\mathrm{CW}} = \frac{1}{2} V_p I_{p1} \approx \frac{1}{2} a V_p I_{s1} \tag{33}$$

where V_p is the peak value of the transformer's input voltage, a is the transformer's turns ratio, I_{p1} and I_{s1} are the magnitudes of the fundamental components of transformer primary and secondary nominal currents, respectively.

With an input voltage of $V_p \cos(\omega t + \theta_v)$ on the primary side of the transformer, the maximum output voltage produced by the traditional CW generator is given by:

$$v_{o,\max,\mathrm{CW}} = 2NV_{\mathrm{CW}} - \Delta v_{o,\mathrm{CW}} \tag{34}$$

where V_{CW} is the peak value of the voltage on the secondary side of the transformer, which can be calculated as:

$$V_{\mathrm{CW}} = \left| \underbrace{aV_p e^{j\theta_v}}_{\substack{\text{voltage applied} \\ \text{to the primary}}} - \underbrace{\left(R_s + j\omega L_s\right) I_{s1} e^{j\theta_i}}_{\text{voltage drop across the transformer}} \right| \tag{35}$$

where ($R_s = R_{\mathrm{sec}} + a^2 R_{\mathrm{pri}}$) and ($L_s = L_{\mathrm{sec}} + a^2 L_{\mathrm{pri}}$) are the resistance and the leakage inductance referred to the secondary winding of the transformer, θ_v is the phase angle of the voltage applied to the primary winding, and θ_i is the phase angle of the main AC current.

Substituting (35) in (34) yields:

$$v_{o,\max,\mathrm{CW}} = \left| 2aNV_p e^{j\theta_v} - \underbrace{2N\left(R_s + j\omega L_s\right) I_{s1} e^{j\theta_i}}_{\substack{\text{voltage drop} \\ \text{caused by transformer}}} \right| - \underbrace{\Delta v_{o,\mathrm{CW}}}_{\substack{\text{voltage drop} \\ \text{caused by capacitors}}} \tag{36}$$

and the transformer copper losses are given by:

$$P_{\mathrm{cu,CW}} = \frac{1}{2} R_s I_{s1}^{\ 2} \tag{37}$$

In this paper, the circuit is divided into m shorter (lower number of stages) modules whose outputs are connected in series to reduce the voltage drop across the Cockroft-Walton voltage multiplier. In this arrangement, the inputs of these modules must be fed by m-isolated sources. This can be achieved by using multiple power suppliers feeding multiple isolation transformers (method 1) such that each transformer has a rated power of $S_{r,\mathrm{CW}}/m$ and supplied by the same input voltage of the conventional Cockroft-Walton voltage multiplier, V_p, which in turn reducing the weight, size, and cost of each transformer. Since the magnitude of the fundamental component of each transformer's secondary nominal current is I_{s1}/m, the resistance and the leakage inductance of that transformer equivalent to the secondary winding is expected to increase by a factor of x ($x \approx m$), according to wire size specifications.

- Resistance referred to the secondary winding of each transformer becomes $mR_{\mathrm{sec}} + a^2 mR_{\mathrm{pri}}$.
- Leakage inductance referred to the secondary winding of each transformer becomes $mL_{\mathrm{sec}} + a^2 mL_{\mathrm{pri}}$.

For example, assume that the rated secondary current of the transformer used in the conventional Cockroft-Walton is 5 A. From the wire size specifications, the conductor size is 0.52 mm^2 [13]. If the circuit is divided into 10 modules

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(m = 10), the rated current of each transformer is 0.5 A. In this case, the conductor size is 0.05 mm^2 [13]. As a result, the transformer's resistance will increase by a factor of 10.4. Since the transformer's inductance is inversely proportional to the transformer's rated current, according to Ampere's law, it will increase by a factor of 10.

On the other hand, the input power stage can be also replaced by multiple isolated windings on the secondary side of a single transformer, called multiphase transformer (method 2). The magnitude of the fundamental component of each winding's secondary current will be I_{s1}/m. With a rated secondary current of I_{s1}/m, the resistance and leakage inductance of each secondary winding will increase by a factor x ($x \approx m$):

- Resistance equivalent to each secondary winding of the multiphase transformer becomes $mR_{\text{sec}} + a^2R_{\text{pri}}$.
- Leakage inductance equivalent to each secondary winding of the multiphase transformer becomes $mL_{\text{sec}} + a^2L_{\text{pri}}$.

Multiphase transformer with custom made core and optimized core materials for feeding modular HV multipliers is going to be the focus of our next research. The proposed circuit just aims to increase the maximum output voltage of the HVDC multiplier significantly, in comparison with the conventional multipliers.

The maximum output voltage provided by each module in the proposed generator can be represented as:

$$v_{o,\max} = 2NV - \Delta v_o \tag{38}$$

where V is the peak value of the secondary voltage that feeds each module in the proposed generator. Both feeding methods produce the same value of V, which is given by (see appendix A1):

$$V = \left| \left(aV_P e^{j\theta_v} - \left(R_s + j\omega L_s \right) I_{s1} e^{j\theta_i} \right) \right| \tag{39}$$

Substituting (39) in (38) yields:

$$v_{o,\max} = \left| 2aNV_P e^{j\theta_v} - 2N\left(R_s + j\omega L_s \right) I_{s1} e^{-j\theta_i} \right| - \underbrace{\Delta v_o}_{< \Delta v_{o,\text{CW}}} > v_{o,\max,\text{CW}} \tag{40}$$

The total copper losses absorbed by transformer(s) are the same for both methods and can be calculated as (see appendix A2):

$$P_{\text{cu}} = \frac{1}{2} R_s I_{s1}^{\ 2} \tag{41}$$

Comparing (36) with (40) and (37) with (41) show that, under the same load current and source frequency conditions and with the same number of capacitors and diodes, the proposed topology is able to generate higher output voltages (at the cost of adding isolation transformers or using a multiphase transformer). However, the copper losses and voltage drop along the transformer(s) is quite similar in both topologies regardless of which method is used to feed the modules. Derivations of (40) and (41) are given in appendices A1 and A2.

III. Simulation Results

To demonstrate the main characteristics of the proposed generator, the circuit has been simulated using Matlab/Simulink. In this simulation, the Cockroft-Walton circuit has 12 stages (N = 12) with capacitances, all equal to 0.05 μF. The peak value of the source is 100 kV at a frequency of 150 Hz. The load current to be supplied by the generator is 5 mA. The converter is tested for different number of SMs and stages such that the total number of elements is fixed: (m = 2, n = 6), (m = 3, n = 4), (m = 4, n = 3), and (m = 6, n = 2).

Fig. 4 shows the simulated output voltages of the converter and their AC components when m = 2, m = 3, m = 4, and m = 6. In this simulation, the modules of the generator are supplied using method 1. It is clear that, when m increases, the output voltage increases, which results in lower regulation factor and higher DC output voltage for the same AC supply voltage as shown in Fig. 5. The ripple factor of the output voltage decreases when m increases since the fundamental frequency of the harmonics is increased.

The frequency spectrum of the output voltages is shown in Fig. 6 for different number of stages and modules. When m = 2 (even), the harmonics appear at 2f and its multiples, that is, at frequencies 2f, 4f, 6f, and so on. However, when m = 3 (odd), the harmonics appear at 3f, 6f, 9f, and so on. It is clear that, when m is even integer, only even harmonics are present and the odd harmonics disappear from the waveform of output voltage.

Fig. 7 shows the simulated output voltages of the converter and their AC components for different number of stages and modules in the case of equal phases of input sources (method 2). It is clear that, when m increases, the output voltage increases which results in lower regulation factor and higher DC output voltage for the same AC supply voltage. The ripple factor of the output voltage decreases when m increases since the peak value of AC component is reduced. It can be observed that, this method produces a level of harmonic distortion of the output voltages higher than that of the balanced phases technique (method 1) with the same regulation factor for every m. However, this method produces a level of ripple content of the output voltages lower than that of the ripple produced by the traditional CW circuit with lower voltage drop.

Fig. 8 shows the effect of variations of generator capacitance on the voltage drop at the output of the proposed generator for different number of stages and SMs at constant frequency and load current. It is clear that, small values of generator capacitance can be used to produce the same voltage drop of CW circuit (m = 1, n = 12). The capacitance decreases by an amount of 0.048 μF when the number of SMs is 6 and the number of stages/SM is 2. Table I summarizes the new values of the generator capacitance for the same voltage drop and different number of SMs and stages.

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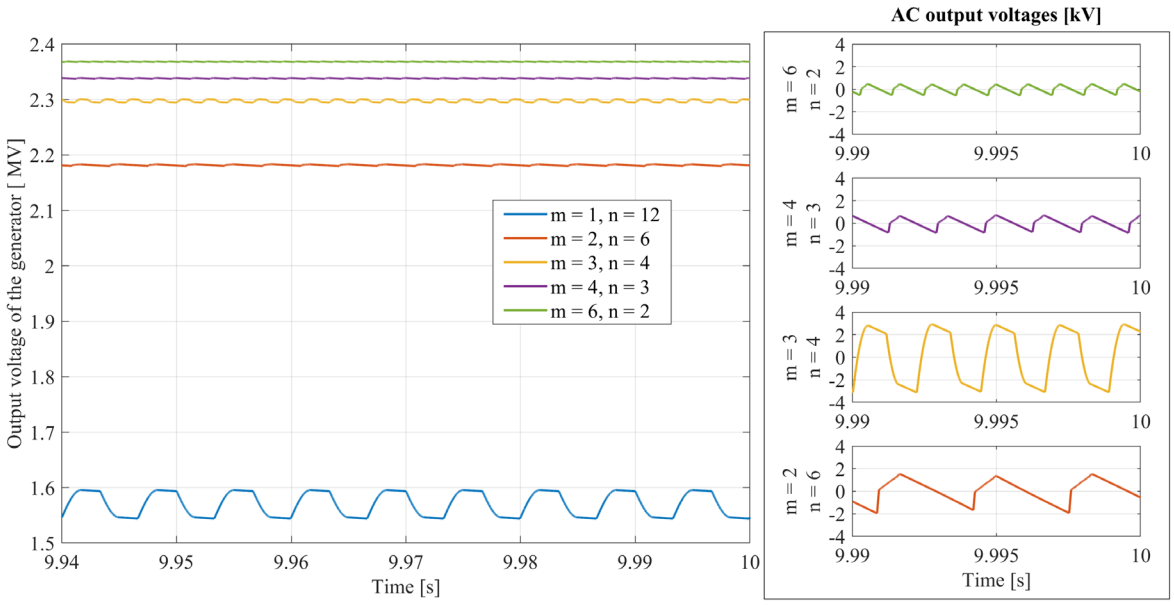

Fig. 4. The steady state output voltages of the generator and their AC components.

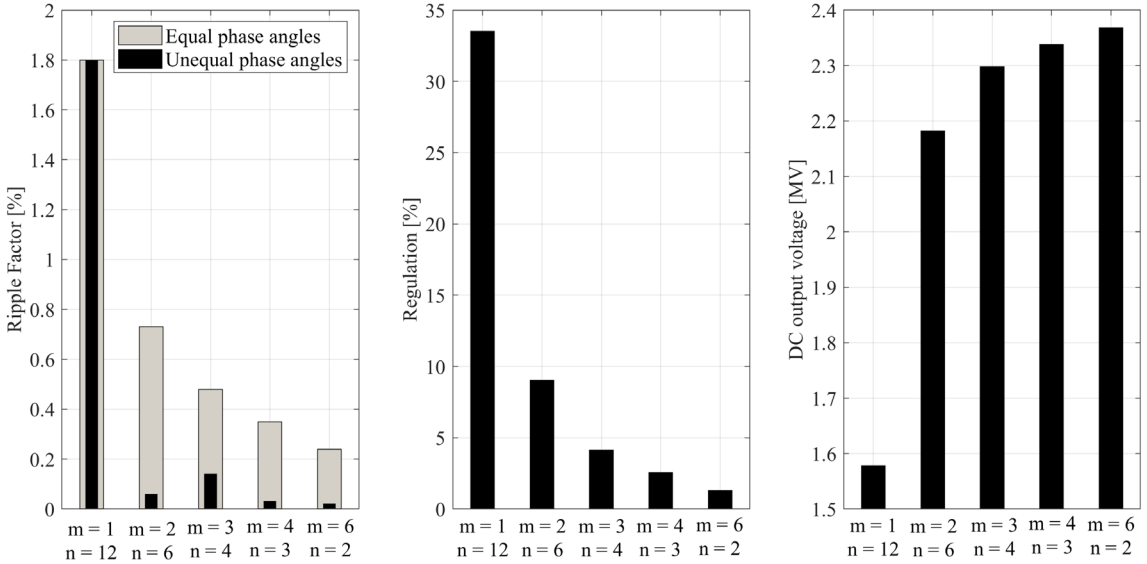

Fig. 5. The mean value of the output voltage, regulation and ripple factor for different number of stages and modules.

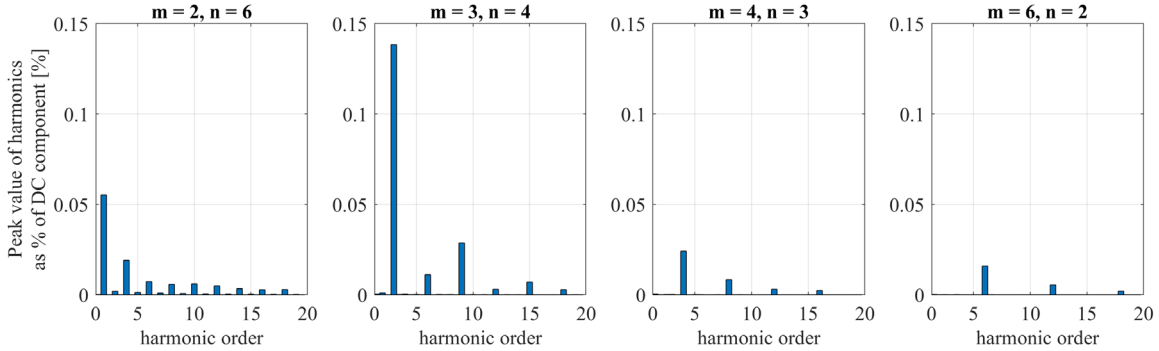

Fig. 6. The frequency spectrum of the output voltages for different number of stages and modules.

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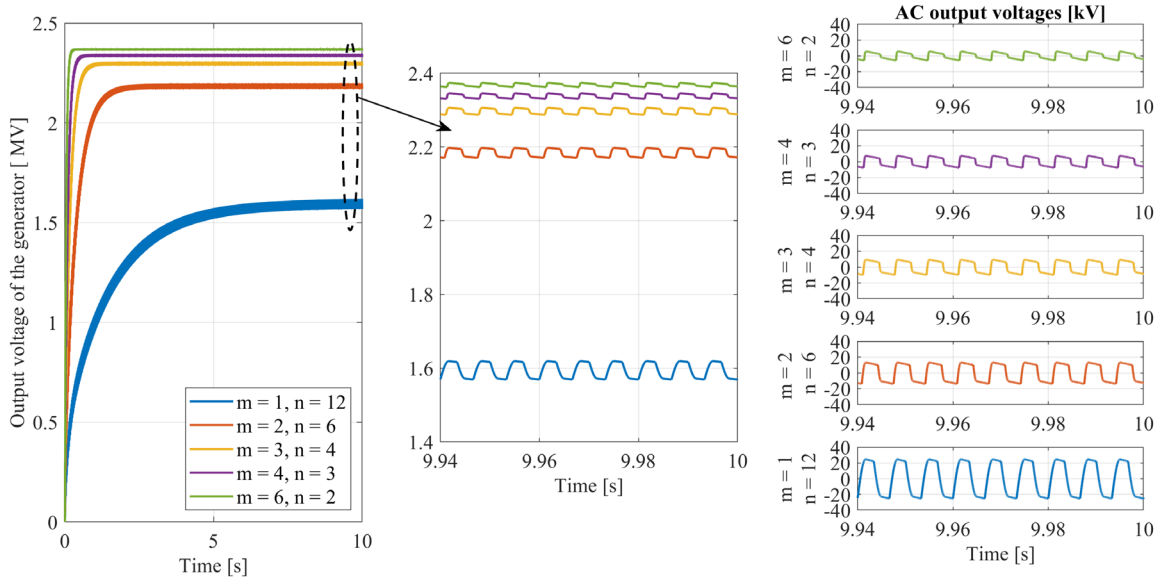

Fig. 7. The output voltages of the generator and their AC components in the case of equal phases of input sources.

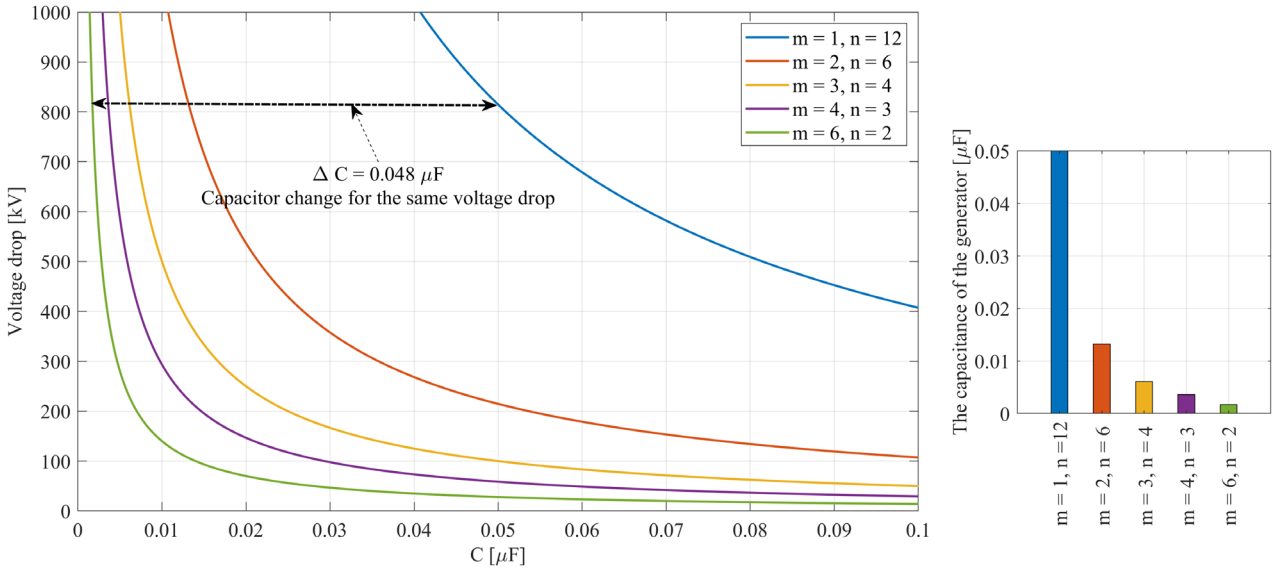

Fig. 8. The voltage drop versus C, and the new values of C for different number of stages and modules.

TABLE I
CAPACITANCE OF THE GENERATOR FOR THE SAME VOLTAGE DROP AND DIFFERENT NUMBER OF SMS AND STAGES

Δv_o [kV]	C [μF]	C' [μF]	m	n	$N = mn$
814.7	0.05	0.0500	1	12	12
814.7	0.05	0.0132	2	6	12
814.7	0.05	0.0061	3	4	12
814.7	0.05	0.0036	4	3	12
814.7	0.05	0.0017	6	2	12

To verify the performance of the proposed generator, the ripple and regulation factors have been compared to the standard CW-HVDC system in [12]. The CW-HVDC system has 20 stages (N = 20) with capacitances, all equal to 13 μF. The peak value of the source is 17 kV at a frequency of 5 kHz. The load current to be supplied by the generator is 6.2 A. The proposed generator is tested for different number of SMs and stages such that the total number of elements is fixed and the number of SMs is even: (m = 2, n = 10), (m = 4, n = 5), and (m = 10, n = 2).

Fig. 9 shows the output voltages of the CW-HVDC system with its AC component. The figure also shows the simulated output voltages of the proposed converter and their AC

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components when $m = 2$, $m = 4$, and $m = 10$. In this simulation, the modules of the proposed generator are supplied using method 1 (balanced input sources). It is clear that, the proposed generator provides better voltage regulation and ripple factors than do conventional CW-multiplier chain circuits. Table II summarizes the ripple and regulation factors, which are obtained by the proposed generator and the traditional CW-HVDC system.

Additionally, the output voltage increases when m increases, which results in lower regulation factor and higher DC output voltage for the same AC supply voltage. The ripple factor of the output voltage decreases when m increases since the fundamental frequency of the harmonics is increased.

Fig. 10 shows the simulated output voltages of the converter and their AC components for different number of stages and modules in the case of equal phases of input sources (method 2). It is clear that, when m increases, the output voltage increases which results in lower regulation factor and higher DC output voltage for the same AC supply voltage. The ripple factor of the output voltage decreases when m increases since the peak value of AC component is reduced. It can be observed that, this method produces a level of harmonic distortion of the output voltages higher than that of the balanced phases technique (method 1) with the same regulation factor for every m. However, this method produces a level of ripple content of the output voltages lower than that of the ripple produced by the traditional CW circuit with lower voltage drop.

Fig. 11 shows the reduction of generator capacitance for different number of stages and SMs if the proposed generator is designed to produce the same voltage drop of CW-HVDC given in [12]. It is clear that, small values of generator capacitance can be used to produce the same voltage drop of CW circuit with direct benefits on the ripple factor. The minimum internal capacitance of the proposed circuit is 0.165 µF compared to 13 µF necessary for the generator proposed in [12], which is relatively low and provides for better ripple factor than do conventional rectifier-multiplier chain circuits.

TABLE II
COMPARISON WITH CW-HVDC SYSTEM, PROPOSED IN [12]

	Topology	m	n	Peak-to-peak ripple voltage [kV]	Maximum output voltage [kV]	Ripple factor [%]	Regulation factor [%]
	CW-HVDC System [12]	1	20	20	200	10	70.06
Method 1	Proposed HVDC generator	2	10	0.6	532	0.3	20.36
	Proposed HVDC generator	4	5	0.3	632	0.15	5.39
	Proposed HVDC generator	10	2	0.1	660	0.05	1.20
Method 2	Proposed HVDC generator	2	10	10	532	5	20.36
	Proposed HVDC generator	4	5	5.8	632	2.9	5.39
	Proposed HVDC generator	10	2	2.6	660	1.3	1.20

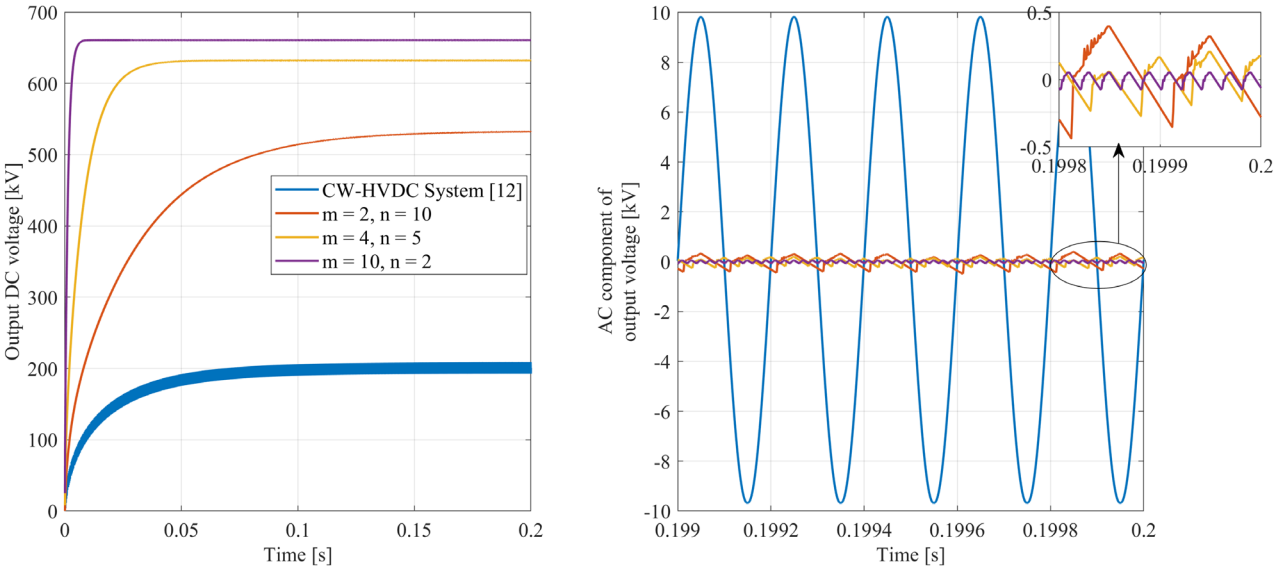

Fig. 9. The output voltages of the proposed generator and the CW-HVDC system given in [12] and their AC components in the case of balanced input sources.

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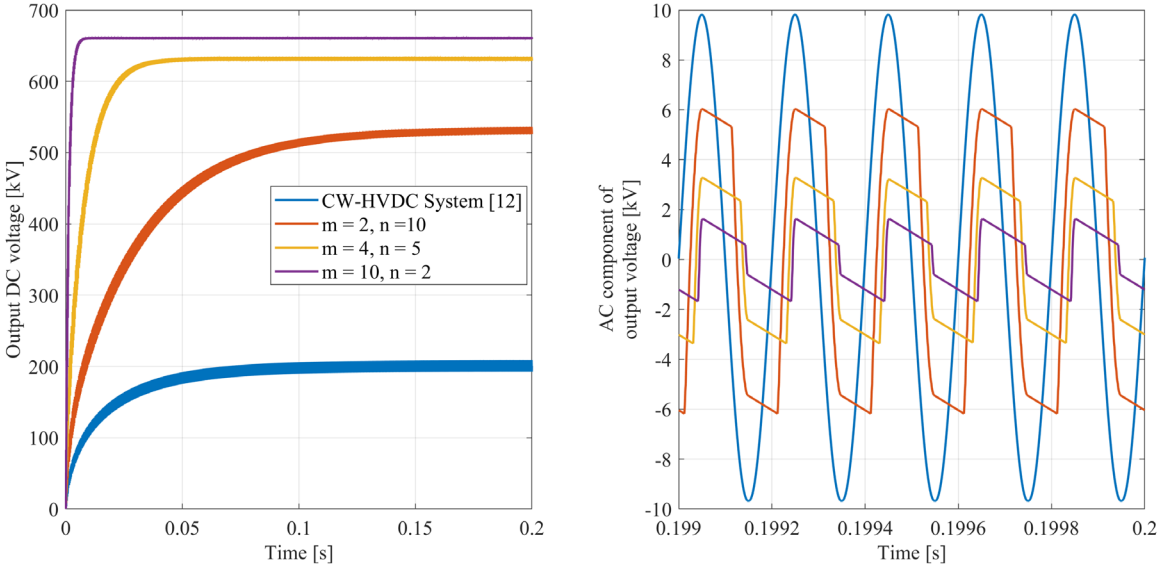

Fig. 10. The output voltages of the proposed generator and the CW-HVDC system given in [12] and their AC components in the case of equal phases of input sources.

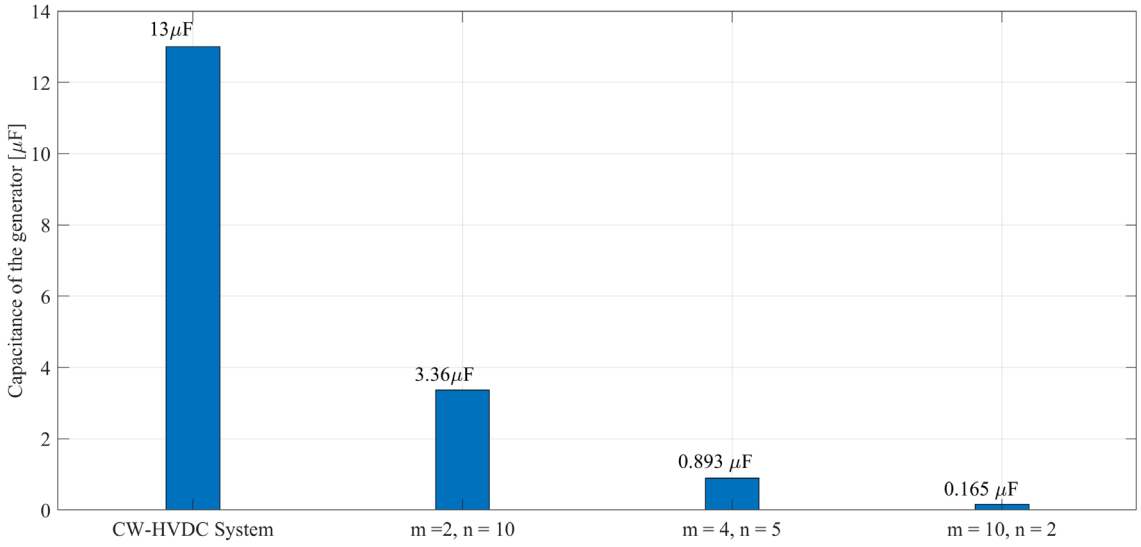

Fig. 11. Capacitance of the CW-HVDC system and the proposed generator for different number of modules and stages.

IV. Experimental Results

The proposed generator has been experimentally tested on a small-scale laboratory prototype. In order to reduce the complexity of the circuit, the generator is constructed with 1-SM and 12 stages, 2-SMs and 6 stages/SM, and 3-SMs and 4 stages/SM. A photograph of the generator with three SMs built in the laboratory is shown in Fig. 12.

The prototype of the generator has been operated with a static resistive load to verify the effectiveness of reducing both ripple and regulation factors. The circuit parameters used for this experiment are summarised in Table III. For comparison purposes, numerical simulations have been carried out using the same circuit parameters used for the experiment.

Fig. 13 shows both simulated and experimental waveforms of the load voltage for different number of SMs. In this experiment, the modules are supplied using method 1 such

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that the sources are shifted from each other by 1200 and 1800 when m is 3 and 2, respectively. Fig. 14 shows both simulated and experimental waveforms of the AC component of the load voltage and the output ripple factor when the number of SMs is 1, 2, and 3. The results show that, although the generator has low number of SMs, the ripple is small, as predicted by the simulations. The lowest RF has been obtained when $m = 2$ since the odd harmonics disappeared from the waveform of output voltage.

Fig. 15 shows the mean value of the output voltage and the regulation factor for different number of SMs and stages. It is clear that, when m increases, the output voltage increases which results in lower regulation factor and higher DC output voltage for the same AC supply voltage. The result in Fig. 13 shows a good agreement between simulated and experimental results.

Fig. 16 shows both simulated and experimental waveforms of the output voltage and its AC component for different number of SMs. In this experiment, the SMs are supplied by isolated AC sources that have the same magnitude, frequency and phase (method 2). The results confirm the correct operations of the generator and the ripple decreases when m increases. It is clear that, a high DC to AC voltage ratio is obtained even though the SMs are fed by sources that have the same phase.

TABLE III
CIRCUIT PARAMETERS USED FOR EXPERIMENT.

Symbol	Quantity	
P	load active power	100 W
V	AC supply voltage	155.5 V
I	Nominal DC current	17.8 mA
f	Nominal AC supply frequency	50 Hz
C	Generator capacitance	330 µF
$N = mn$	Number of modules and stages	12

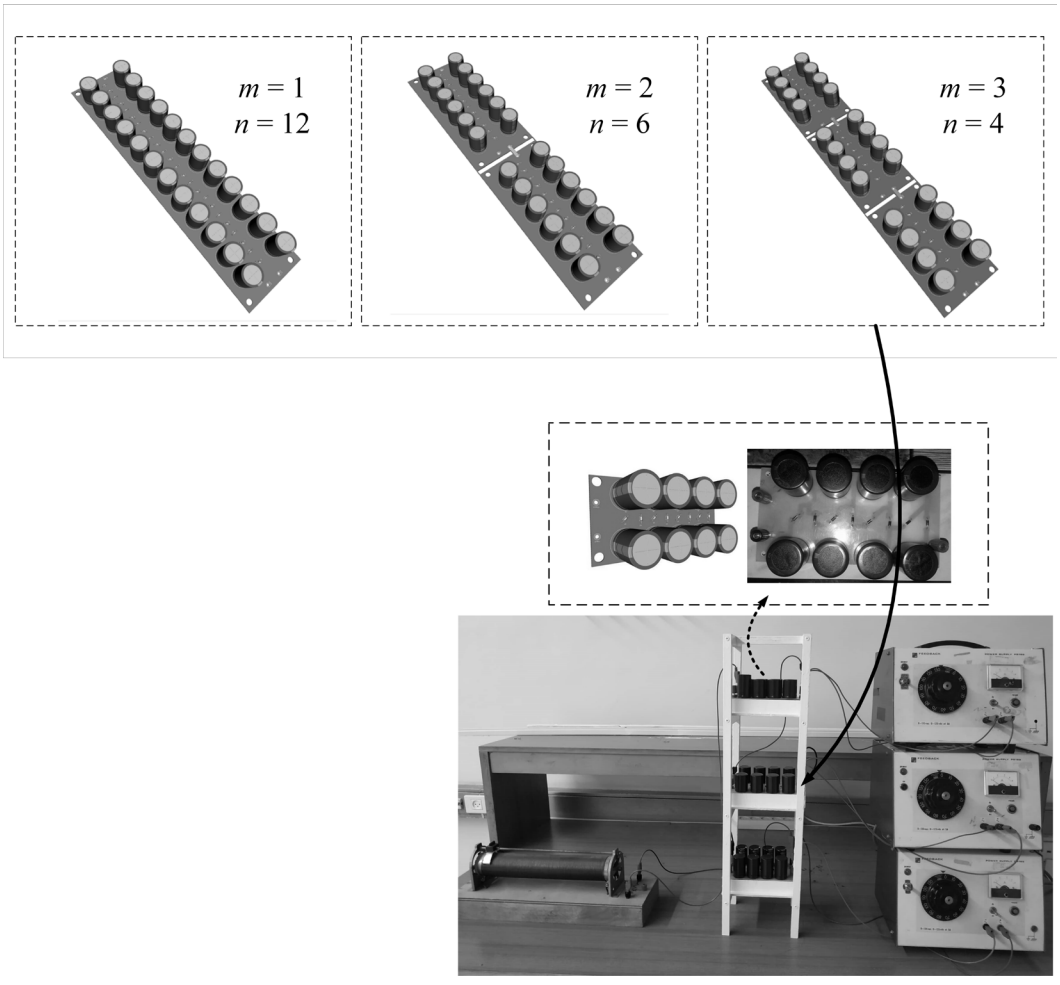

Fig. 12. Prototype of a high voltage DC generator with three SMs.

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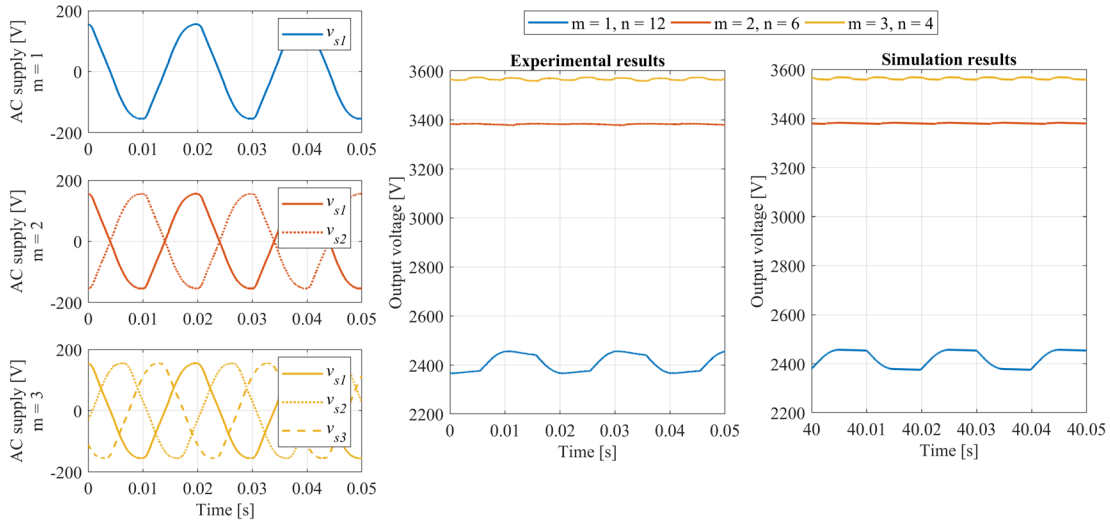

Fig. 13. The AC source voltages and the steady state output voltages of the generator.

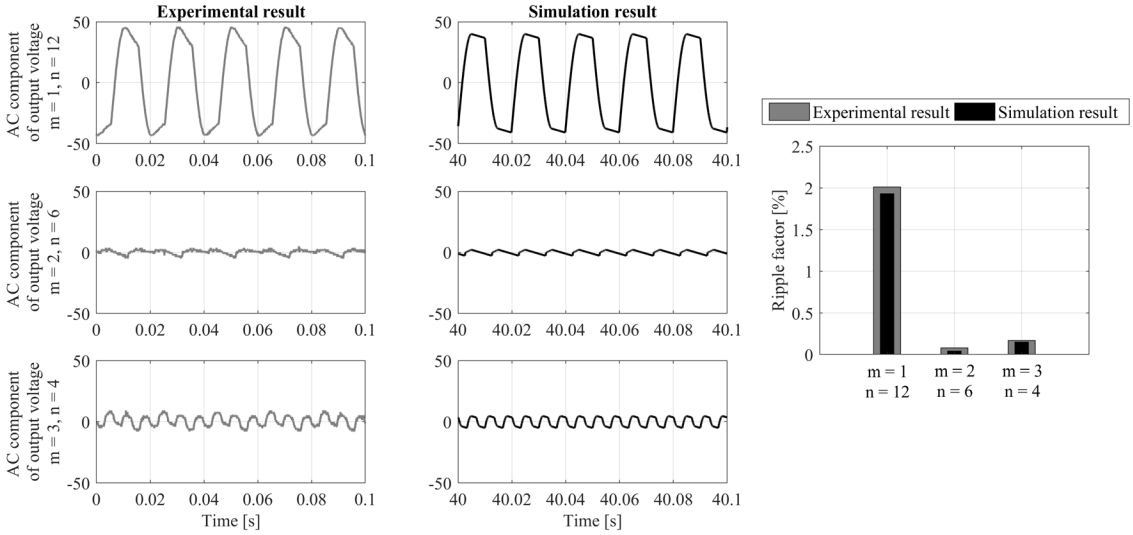

Fig. 14. The steady state AC components of the generator output voltages and the mean values of the output voltage.

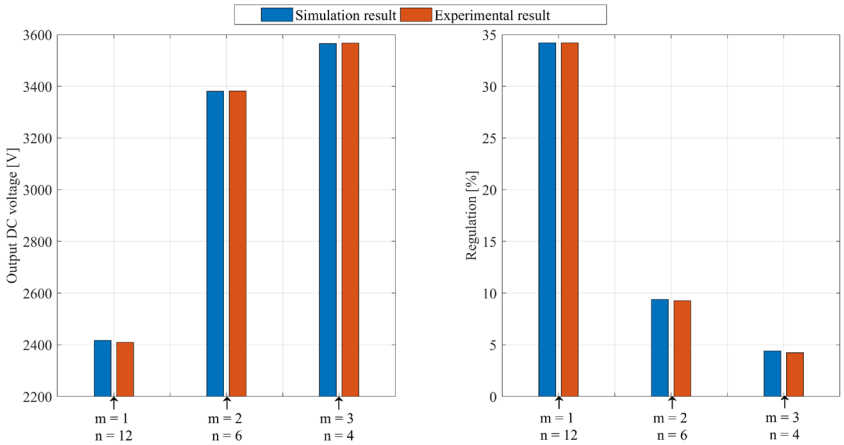

Fig. 15. The mean value of the output voltage and regulation factor for different number of stages and modules.

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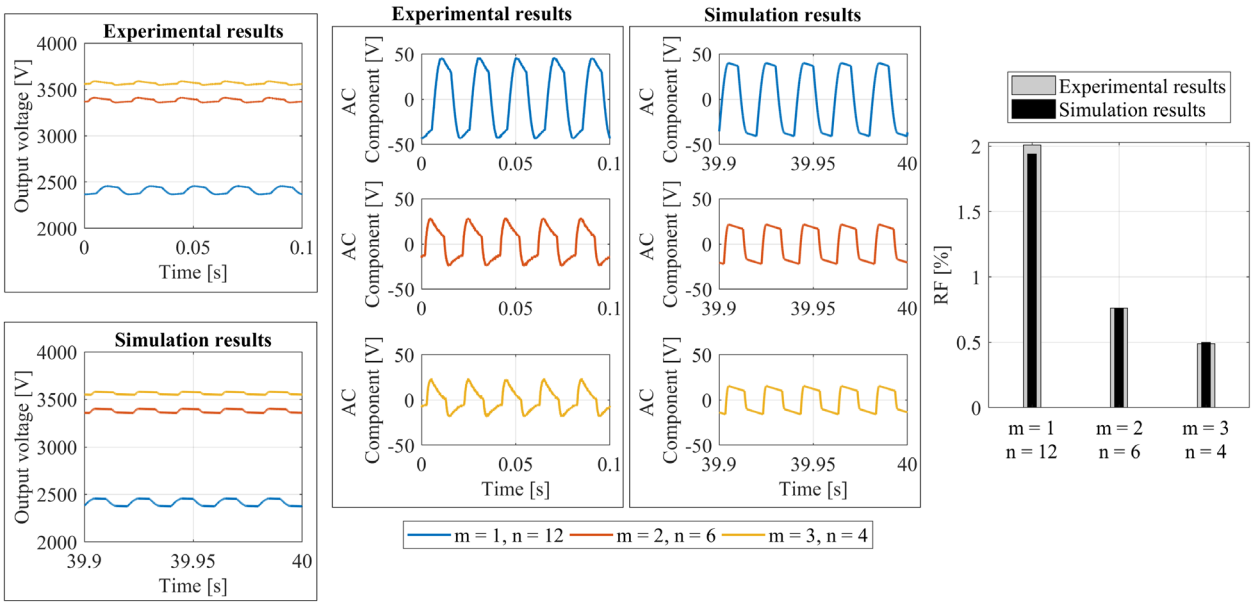

Fig. 16. The output voltages of the generator and their AC components in the case of equal phases of input source.

V. Conclusion

This paper has presented a series connected high voltage multiplier for testing High Voltage Alternating Current (HVAC) power cables based on the topology of modular circuits. Mathematical models for ripple factor, regulation, and harmonic contents of the output DC voltage have been presented in the paper. In comparison with the traditional CW circuit, the proposed circuit produces an extremely lower ripple factor of the output voltage, with direct benefits for the operations with lower regulation factor (< 2 %). As a second advantage, a reduction of stored energy is possible if the proposed generator is constructed to produce the same voltage drop of the traditional CW circuit. The analytical calculations have been verified by numerical simulation and experiment with a comparison of ripple and regulation factors between the traditional CW generator and the proposed generator. Both computer simulations in Matlab/ Simulink and experiments using a laboratory prototype have confirmed the correct operations of the proposed generator and the effectiveness of the number of SMs and stages.

APPENDIX A1 - DERIVATION OF (40)

The peak value of the secondary voltage that feeds each module, when method 1 is used, is derived as follows:

$$V = \left| \left(aV_P e^{j\theta_v} - \left[\left(mR_{\text{sec}} + a^2 mR_{\text{pri}} \right) + j\omega \left(mL_{\text{sec}} + a^2 mL_{\text{pri}} \right) \right] \frac{I_{s1}}{m} e^{j\theta_i} \right) e^{j\varphi_k} \right|$$

$$= \left| \left(aV_P e^{j\theta_v} - \cancel{m} \left[\left(R_{\text{sec}} + a^2 R_{\text{pri}} \right) + j\omega \left(L_{\text{sec}} + a^2 L_{\text{pri}} \right) \right] \frac{I_{s1}}{\cancel{m}} e^{j\theta_i} \right) e^{j\varphi_k} \right| = \left| aV_P e^{j\theta_v} - \left[\underbrace{\left(R_{\text{sec}} + a^2 R_{\text{pri}} \right)}_{R_s} + j\omega \underbrace{\left(L_{\text{sec}} + a^2 L_{\text{pri}} \right)}_{L_s} \right] I_{s1} e^{j\theta_i} \right| \quad \text{(A1.1)}$$

$$= \left| aV_P e^{j\theta_v} - \left(R_s + j\omega L_s \right) I_{s1} e^{j\theta_i} \right|$$

where θ_v is the phase angle of the voltage applied to the primary winding within the first module, θ_i is the phase angle of the main current feeding the first module, and φ_k is the phase angle of the secondary voltage applied to k-th module, which is $2\pi\ (k-1)/m$,

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The peak value of the secondary voltage that feeds each module, when method 2 is used, is derived as follows:

$$V = \left| aV_P e^{j\theta_v} - \left[\left((mR_{\text{sec}}) + j\omega (mL_{\text{sec}}) \right) \frac{I_{s1}}{m} e^{j\theta_i} \right] - \left[\left(a^2 R_{\text{pri}} + j\omega a^2 L_{\text{pri}} \right) I_{s1} e^{j\theta_i} \right] \right|$$

$$= \left| aV_P e^{j\theta_v} - \left[\cancel{m} \left(R_{\text{sec}} + j\omega L_{\text{sec}} \right) \frac{I_{s1}}{\cancel{m}} e^{j\theta_i} \right] - \left[\left(a^2 R_{\text{pri}} + j\omega a^2 L_{\text{pri}} \right) I_{s1} e^{j\theta_i} \right] \right| = \left| aV_P e^{j\theta_v} - \left[\underbrace{\left(R_{\text{sec}} + a^2 R_{\text{pri}} \right)}_{R_s} + j\omega \underbrace{\left(L_{\text{sec}} + a^2 L_{\text{pri}} \right)}_{L_s} \right] I_{s1} e^{j\theta_i} \right| \quad \text{(A1.2)}$$

$$= \left| aV_P e^{j\theta_v} - \left(R_s + j\omega L_s \right) I_{s1} e^{j\theta_i} \right|$$

where θ_v is the phase angle of the voltage applied to the primary winding of multiphase transformer and θ_i is the phase angle of the main current feeding each module in the circuit.

APPENDIX A2 - DERIVATION OF (41)

The total copper losses in the multiple transformers, when method 1 is used, is derived as follows:

$$P_{\text{cu}} = \underbrace{\frac{1}{2}(mR_s)\left(\frac{I_{s1}}{m}\right)^2 + \frac{1}{2}(mR_s)\left(\frac{I_{s1}}{m}\right)^2 + \cdots + \frac{1}{2}(mR_s)\left(\frac{I_{s1}}{m}\right)^2}_{m \text{ times}} = \frac{1}{2} R_s {I_{s1}}^2 \quad \text{(A2.1)}$$

and the total copper losses absorbed by the multiphase transformer, when method 2 is used, is derived as follows:

$$P_{\text{cu}} = \underbrace{\frac{1}{2}(mR_{\text{sec}})\left(\frac{I_{s1}}{m}\right)^2 + \frac{1}{2}(mR_{\text{sec}})\left(\frac{I_{s1}}{m}\right)^2 + \cdots + \frac{1}{2}(mR_{\text{sec}})\left(\frac{I_{s1}}{m}\right)^2}_{m \text{ times}} + \frac{1}{2}\left(a^2 R_{\text{pri}}\right) {I_{s1}}^2 = \frac{1}{2}\left(R_{\text{sec}} + a^2 R_{\text{pri}}\right) {I_{s1}}^2 = \frac{1}{2} R_s {I_{s1}}^2 \quad \text{(A2.2)}$$

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