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Research Article

Reduced Voltage Scaling in Clock Distribution Networks

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We propose a novel circuit technique to generate a reduced voltage swing (RVS) signals for active power reduction on main buses and clocks. This is achieved without performance degradation, without extra power supply requirement, and with minimum area overhead. The technique stops the discharge path on the net that is swinging low at a certain voltage value. It reduces active power on the target net by as much as 33% compared to traditional full swing signaling. The logic 0 voltage value is programmable through control bits. If desired, the reduced-swing mode can also be disabled. The approach assumes that the logic 0 voltage value is always less than the threshold voltage of the nMOS receivers, which eliminate the need of the low to high voltage translation. The reduced noise margin and the increased leakage on the receiver transistors using this approach have been addressed through the selective usage of multithreshold voltage (MTV) devices and the programmability of the low voltage value.

1. Introduction

Continuous VLSI technology scaling has enabled integration of millions of transistors on a single chip working in over GHz clock frequencies. Besides area (cost) and performance, modern VLSI designs are critical to achieve low-power consumption due to limited battery lifetime in mobile applications, increased priority to achieve improved energy efficiency for data centers, web servers, supercomputing centers, and expensive alternative cooling options for personal computers.

LVS is an effective active power consumption reduction technique since active power consumption is proportional to signal voltage swing. Interconnects are responsible for up to 50% of the active power consumption, while up to 90% of interconnect power consumption comes from only 10% of the interconnects, such as clock networks and global signal busses [1]. Developing LVS techniques for these powers hungry interconnects are critical to modern VLSI designs.

Power efficiency is an increasingly critical VLSI design objective. Low-power design for high-performance computers improves energy efficiency and reduces package cost for heat dissipation, while low-power design for mobile applications increases battery lifetime.

Low-voltage swing is an effective technique to reduce dynamic power consumption, especially for clocks which are among the most active signals in a VLSI circuits and generally consume up to 50% of the total power [2]. Reduced voltage swing clock signals can be applied at the upper level of a clock tree for low-power, while clock gates (such as inverters) amplify the signals to full swing upon reaching sequential elements [1].

Existing techniques to generate reduced voltage swing signals require an extra low-power supply or need precise timing for a pulse signal which enables the driver gate, while a number of voltage level converters have been developed which trigger a reduced voltage swing signal into a full swing signal [3].

In general there are two techniques to reduce clocking swing, the first one is dual power supply voltage the second one is single power supply voltage. The first method adds more complexity to the overall design and layout. The second one, single supply voltage challenge, is the design of reduced swing buffers. Many papers [1, 4] implemented this method by utilizing pMOS for passing low logic level and nMOS for passing high level logic. Such techniques result in poor rise and fall times, which make it impractical for high-performance applications.

Table 1: Comparison of full swing and RVS inverters.

	FVS	RVS
Power (uW)	0.279	0.107
Delay (ps)	0.449	0.394
Rise Slew Rate (ps)	0.074	0.168
Fall Slew Rate (ps)	0.074	0.131

Table 2: Comparison of a clock spine with FVS or RVS clock buffers.

	Delay (ps)	Slew Rate (ps)	Power (mW)
FVS	185	4	3.709
RVS	201	5.2	2.7

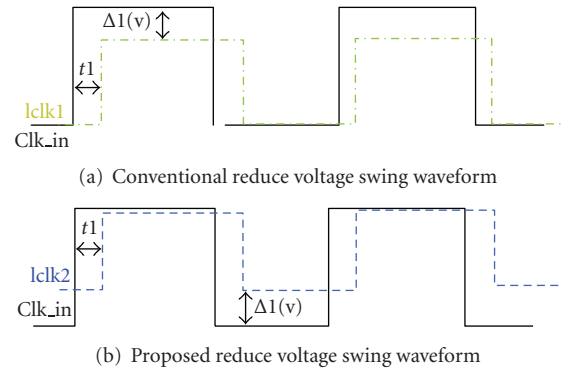

Figure 1: Traditional and new reduce voltage swing waveforms.

In this paper, we propose Reduced Voltage Swing (RVS) design comparing to the traditional Low Voltage Swing (LVS) technique. We elevate the low logic voltage instead of lowering the high logic voltage. We propose an inverter design which generates RVS signals at the cost of an extra transistor, and an extension of the RVS inverter with programmable gates for adjustable low logic voltage. We achieve (1) minimum area overhead (by not requiring an extra power supply network), (2) minimum performance degradation (by keeping the supply voltage and the high logic voltage), and (3) robustness to process variations (the logic 0 voltage is adaptive to process variations). The simulation results from HSPICE [5] tool show that we reduced active power consumption with very limited performance loss.

The rest of the paper is organized as follows. Existing low-voltage swing signal and clocking is presented in Section 2. Section 3 presents the reduce voltage swing principle and circuit followed by implementation and simulation results in Section 4. Finally Section 5 concludes the paper.

2. Existing Low-Voltage Swing Signaling and Clocking Schemes

Existing low-voltage swing circuits [4] process a number of deficiencies, such as the need for extra supplies, performance impact, differential signaling, and reliability degradation. They typically look at reducing the supply voltage on the targeted net, which impacts timing significantly. Most of the papers describing low or reduced voltage swing signals are targeting clock network or signal nodes with high capacitance to reduce power. Zhang et al. [4] surveyed the different options and circuits used to generate small or reduced signal swings. The paper lists the comparison of speed, power, and complexity of the different options. It also points out the deficiencies of each technique. They also proposed their own scheme called pseudodifferential Interconnect (PDIFF). However, all these LVS signaling techniques require an extra power supply which adds cost and complexity to the design.

An LVS clocking technique that requires only a single power supply is proposed [3], wherein intermediate clock buffers are turned off once they reach the desired voltage levels. This makes the clock node essentially floating and is susceptible to noise. Subsequent regular clock buffers act as amplifiers which restore the clock signal to full swing. The short circuit power consumption of these amplifier clock buffers is reduced through the usage of small and high threshold voltage transistors.

3. Reduce Voltage Swing Principle and Circuits

For clock distribution the synchronous clock must be distributed all over the chip with minimum possible skew. The clocking network consumes significant amount of power, Clock distribution interconnects, and their increased parasitic with scaling results in the increased power consumption. Typically, buffers are inserted within the clock network to isolate the downstream capacitance; thus it is reducing the transition times and increases amount of power consumption substantially.

As stated and used in [6–8] there is a need to reduce the power dissipation of the clock network while maintaining the performance objectives. Power can be reduced by reducing Clock frequency. However, the frequency cannot be changed without significant architectural changes. So alternatively, power can be reduced by reducing the total load capacitance, CL, on all nodes, reducing VDD or reducing Vswing, without reducing VDD, which corresponds to a linear reduction in the power dissipation.

The former works on reducing V(swing) via adding extra supplies to the selected nets. Extra supply not only adds cost and area but also increases the complexity of routing and switching off two power grids for power savings.

Figure 1 shows the traditional waveforms obtained with the conventional reduce voltage swing approach. It also shows the waveforms produced by our proposed circuit. The main difference is that with the proposed circuit, the voltage waveform still reaches V_{dd}. This eliminates the timing impact; also the rising edge delay of the lclk1 from clk_in ($t1$) (Figure 1) in our approach is not impacted.

The proposed RVS circuit is shown in Figure 2 with both receiver and driver using the same power supply. We showed both traditional and the new circuit with the expected waveforms. In the proposed approach no extra supply is

Table 3: Simulation comparison with different setup.

	Device width	clkin	Input	Power		Delay (ps)		Slope (ps)			
cap	hvtw	pwidth	voltage (v)	old	new	old	new	old	new	old	new
0	0.25	2.0$E-10$	0.9	active_ power <w>	active_ power <w>	delay_ clkin_ out <ps>	delay_ clkin_ out <ps>	slope_ fall_out <ps>	slope_ out_ fall <ps>	slope_ rise_ out <ps>	slope_ out_ rise <ps>
2.00$E-15$	0.25	2.0$E-10$	0.9	8.7$E-06$	3.9$E-06$	39.93	37.24	4.40	10.66	4.40	13.57
0	0.25	3.0$E-10$	0.9	1.2$E-05$	7.9$E-06$	52.15	42.62	6.55	13.45	6.55	19.41
2.00$E-15$	0.25	3.0$E-10$	0.9	5.7$E-06$	2.6$E-06$	39.99	38.37	4.40	10.66	4.40	13.57
0	0.25	4.0$E-10$	0.9	8.3$E-06$	5.3$E-06$	52.20	45.29	6.55	13.45	6.55	19.41
2.00$E-15$	0.25	4.0$E-10$	0.9	4.3$E-06$	1.9$E-06$	40.01	38.86	4.40	10.66	4.40	13.57
0	0.25	5.0$E-10$	0.9	5.9$E-06$	4.0$E-06$	52.22	46.37	6.55	13.45	6.55	19.42
2.00$E-15$	0.25	5.0$E-10$	0.9	3.5$E-06$	1.6$E-06$	40.02	39.17	4.40	10.66	4.40	13.59
0	0.25	6.0$E-10$	0.9	5.1$E-06$	3.2$E-06$	52.23	47.03	6.55	13.45	6.55	19.43
2.00$E-15$	0.25	6.0$E-10$	0.9	3.2$E-06$	1.3$E-06$	40.03	39.40	4.40	10.66	4.40	13.59
0	0.25	2.0$E-10$	1	4.3$E-06$	2.6$E-06$	52.24	47.51	6.55	13.45	6.55	19.43
2.00$E-15$	0.25	2.0$E-10$	1	1.2$E-05$	4.8$E-06$	33.93	31.31	3.98	9.87	3.98	10.57
0	0.25	3.0$E-10$	1	1.6$E-05$	9.8$E-06$	44.57	36.89	5.90	12.61	5.90	14.98
2.00$E-15$	0.25	3.0$E-10$	1	7.6$E-06$	3.2$E-06$	33.95	32.22	3.98	9.87	3.98	10.59
0	0.25	4.0$E-10$	1	1.1$E-05$	6.5$E-06$	44.59	39.01	5.90	12.61	5.90	14.96
2.00$E-15$	0.25	4.0$E-10$	1	5.7$E-06$	2.4$E-06$	33.96	32.63	3.98	9.87	3.98	10.58
0	0.25	5.0$E-10$	1	7.7$E-06$	4.9$E-06$	44.60	39.89	5.90	12.61	5.90	14.98
2.00$E-15$	0.25	5.0$E-10$	1	4.7$E-06$	1.9$E-06$	33.96	32.89	3.98	9.87	3.98	10.58
0	0.25	6.0$E-10$	1	6.7$E-06$	3.9$E-06$	44.60	40.44	5.90	12.61	5.90	14.97
2.00$E-15$	0.25	6.0$E-10$	1	4.2$E-06$	1.6$E-06$	33.96	33.07	3.98	9.87	3.98	10.58
0	0.25	2.0$E-10$	1.1	5.6$E-06$	3.3$E-06$	44.61	40.83	5.90	12.61	5.90	14.96
2.00$E-15$	0.25	2.0$E-10$	1.1	1.5$E-05$	5.8$E-06$	29.96	27.28	3.73	9.45	3.73	8.91
0	0.25	3.0$E-10$	1.1	2.1$E-05$	1.2$E-05$	39.49	32.98	5.49	12.25	5.49	12.43
2.00$E-15$	0.25	3.0$E-10$	1.1	1.0$E-05$	3.9$E-06$	29.97	28.07	3.73	9.45	3.73	8.88
0	0.25	4.0$E-10$	1.1	1.4$E-05$	7.9$E-06$	39.49	34.80	5.49	12.25	5.49	12.43
2.00$E-15$	0.25	4.0$E-10$	1.1	7.6$E-06$	2.9$E-06$	29.97	28.43	3.73	9.45	3.73	8.87
0	0.25	5.0$E-10$	1.1	1.0$E-05$	5.9$E-06$	39.49	35.56	5.49	12.25	5.49	12.43
2.00$E-15$	0.25	5.0$E-10$	1.1	6.2$E-06$	2.3$E-06$	29.97	28.65	3.73	9.45	3.73	8.88
0	0.25	6.0$E-10$	1.1	8.6$E-06$	4.8$E-06$	39.49	36.04	5.49	12.25	5.49	12.43
2.00$E-15$	0.25	6.0$E-10$	1.1	5.6$E-06$	1.9$E-06$	29.97	28.81	3.73	9.45	3.73	8.89
0	0.25	2.0$E-10$	1.2	7.2$E-06$	4.0$E-06$	39.49	36.38	5.49	12.25	5.49	12.42
2.00$E-15$	0.25	2.0$E-10$	1.2	2.0$E-05$	7.0$E-06$	27.33	24.43	3.57	9.18	3.57	7.90
0	0.25	3.0$E-10$	1.2	2.7$E-05$	1.4$E-05$	36.05	30.19	5.26	12.06	5.26	10.94
2.00$E-15$	0.25	3.0$E-10$	1.2	1.3$E-05$	4.6$E-06$	27.34	25.13	3.57	9.18	3.57	7.91
0	0.25	4.0$E-10$	1.2	1.8$E-05$	9.5$E-06$	36.05	31.81	5.26	12.06	5.26	10.91
2.00$E-15$	0.25	4.0$E-10$	1.2	9.9$E-06$	3.5$E-06$	27.34	25.46	3.57	9.18	3.57	7.91
0	0.25	5.0$E-10$	1.2	1.3$E-05$	7.1$E-06$	36.05	32.50	5.26	12.06	5.26	10.93
2.00$E-15$	0.25	5.0$E-10$	1.2	8.2$E-06$	2.8$E-06$	27.34	25.66	3.57	9.18	3.57	7.91
0	0.25	6.0$E-10$	1.2	1.1$E-05$	5.7$E-06$	36.05	32.93	5.26	12.06	5.26	10.94
2.00$E-15$	0.25	6.0$E-10$	1.2	7.4$E-06$	2.3$E-06$	27.34	25.79	3.57	9.18	3.57	7.90
0	0.25	2.0$E-10$	1.3	9.3$E-06$	4.7$E-06$	36.05	33.23	5.26	12.06	5.26	10.94

Table 3: Continued.

	Device width	clkin	Input	Power		Delay (ps)		Slope (ps)			
cap	hvtw	pwidth	voltage (v)	old	new	old	new	old	new	old	new
2.00$E-15$	0.25	2.0$E-10$	1.3	2.6$E-05$	8.2$E-06$	25.60	22.32	3.53	8.85	3.53	7.30
0	0.25	3.0$E-10$	1.3	3.4$E-05$	1.7$E-05$	33.69	28.06	5.11	11.92	5.11	10.00
2.00$E-15$	0.25	3.0$E-10$	1.3	1.7$E-05$	5.5$E-06$	25.60	22.95	3.53	8.85	3.53	7.28
0	0.25	4.0$E-10$	1.3	2.3$E-05$	1.1$E-05$	33.69	29.55	5.11	11.92	5.11	9.97
2.00$E-15$	0.25	4.0$E-10$	1.3	1.3$E-05$	4.1$E-06$	25.60	23.24	3.53	8.85	3.53	7.27
0	0.25	5.0$E-10$	1.3	1.6$E-05$	8.3$E-06$	33.69	30.18	5.11	11.92	5.11	10.00
2.00$E-15$	0.25	5.0$E-10$	1.3	1.1$E-05$	3.3$E-06$	25.60	23.42	3.53	8.85	3.53	7.26
0	0.25	6.0$E-10$	1.3	1.4$E-05$	6.7$E-06$	33.69	30.56	5.11	11.92	5.11	10.01
2.00$E-15$	0.25	6.0$E-10$	1.3	9.6$E-06$	2.7$E-06$	25.60	23.54	3.53	8.85	3.53	7.26
0	0.25	2.0$E-10$	1.4	1.2$E-05$	5.6$E-06$	33.69	30.83	5.11	11.92	5.11	10.01
2.00$E-15$	0.25	2.0$E-10$	1.4	3.4$E-05$	9.5$E-06$	24.48	20.70	3.49	8.46	3.49	6.91
0	0.25	3.0$E-10$	1.4	4.3$E-05$	1.9$E-05$	32.08	26.34	5.10	11.77	5.10	9.41
2.00$E-15$	0.25	3.0$E-10$	1.4	2.3$E-05$	6.3$E-06$	24.48	21.27	3.49	8.46	3.49	6.91
0	0.25	4.0$E-10$	1.4	2.9$E-05$	1.3$E-05$	32.08	27.70	5.10	11.77	5.10	9.40
2.00$E-15$	0.25	4.0$E-10$	1.4	1.7$E-05$	4.8$E-06$	24.48	21.52	3.49	8.46	3.49	6.92
0	0.25	5.0$E-10$	1.4	2.1$E-05$	9.7$E-06$	32.08	28.28	5.10	11.77	5.10	9.40
2.00$E-15$	0.25	5.0$E-10$	1.4	1.4$E-05$	3.8$E-06$	24.48	21.67	3.49	8.46	3.49	6.92
0	0.25	6.0$E-10$	1.4	1.8$E-05$	7.7$E-06$	32.08	28.63	5.10	11.77	5.10	9.40
2.00$E-15$	0.25	6.0$E-10$	1.4	1.3$E-05$	3.2$E-06$	24.48	21.77	3.49	8.46	3.49	6.92
0	0.25	2.0$E-10$	1.5	1.5$E-05$	6.4$E-06$	32.08	28.87	5.10	11.77	5.10	9.40
2.00$E-15$	0.25	2.0$E-10$	1.5	4.3$E-05$	1.1$E-05$	23.76	19.43	3.51	8.01	3.51	6.67
0	0.25	3.0$E-10$	1.5	5.4$E-05$	2.2$E-05$	30.98	24.89	5.07	11.61	5.07	9.05
2.00$E-15$	0.25	3.0$E-10$	1.5	2.9$E-05$	7.3$E-06$	23.76	19.92	3.51	8.01	3.51	6.67
0	0.25	4.0$E-10$	1.5	3.7$E-05$	1.5$E-05$	30.98	26.13	5.07	11.61	5.07	9.04
2.00$E-15$	0.25	4.0$E-10$	1.5	2.2$E-05$	5.5$E-06$	23.76	20.13	3.51	8.01	3.51	6.67
0	0.25	5.0$E-10$	1.5	2.6$E-05$	1.1$E-05$	30.98	26.66	5.07	11.61	5.07	9.03
2.00$E-15$	0.25	5.0$E-10$	1.5	1.8$E-05$	4.4$E-06$	23.76	20.26	3.51	8.01	3.51	6.67
0	0.25	6.0$E-10$	1.5	2.3$E-05$	8.9$E-06$	30.98	26.97	5.07	11.61	5.07	9.02
2.00$E-15$	0.25	6.0$E-10$	1.5	1.6$E-05$	3.6$E-06$	23.76	20.33	3.51	8.01	3.51	6.67
				1.9$E-05$	7.4$E-06$	30.98	27.18	5.07	11.61	5.07	9.01
		Average		2.8$E-07$	1.1$E-07$	0.45	0.39	0.07	0.17	0.07	0.13

needed when generating the RVS signal (lclk2). The overhead of adding a transistor to the driver is very minimal compared to the total net capacitance especially when the driver fans out to many receivers which is true in the clock distribution network or long wire net.

The transistors in our proposed design are with low threshold voltage (LVT) for the driver and high threshold voltage (HVT) for the receiver. This enables a built in noise margin on the net lclk2 which is equal to the voltage difference between the HVT and LVT values. Also the receiver HVT transistor and its drain to source voltage being less than vdd minimize the increased leakage due to elevated gate voltage. The receiver SSTC latch topology [9] is selected because the clock pin goes only into nFET transistor which eliminates the need of level translation to prevent short circuit current. Another advantage of our proposed design is that the lclk2 is always going to be actively driven. In case of coupling noise high on lclk2 net the pull down stack will turn on and clear any charge on the net before it reaches the threshold for the receiver HVT FET. This is true because the driver is LVT and the receiver is HVT device. The addition of series transistor to the final driver slows down the falling edge of the clock which only affect hold time and not the speed of the circuit (clk-> q- delay). The M1 transistor that is controlled by power_mode is meant as an override mode to the system. If power_mode is set to 1, the RVS circuit will behave the same as the traditional one.

One limitation of our proposed technique which shown in Figure 2 is that it only limits the swing of lclk2 between vdd

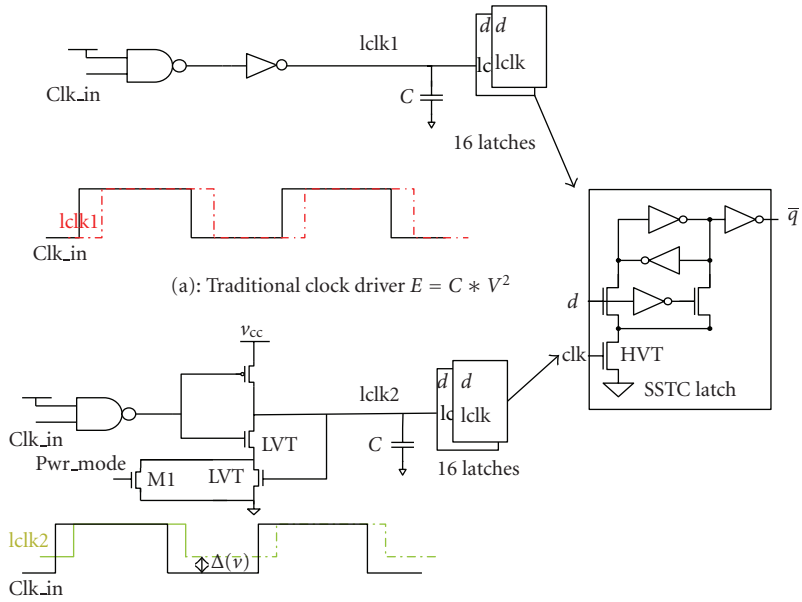

Figure 2: Traditional and new RVS illustration.

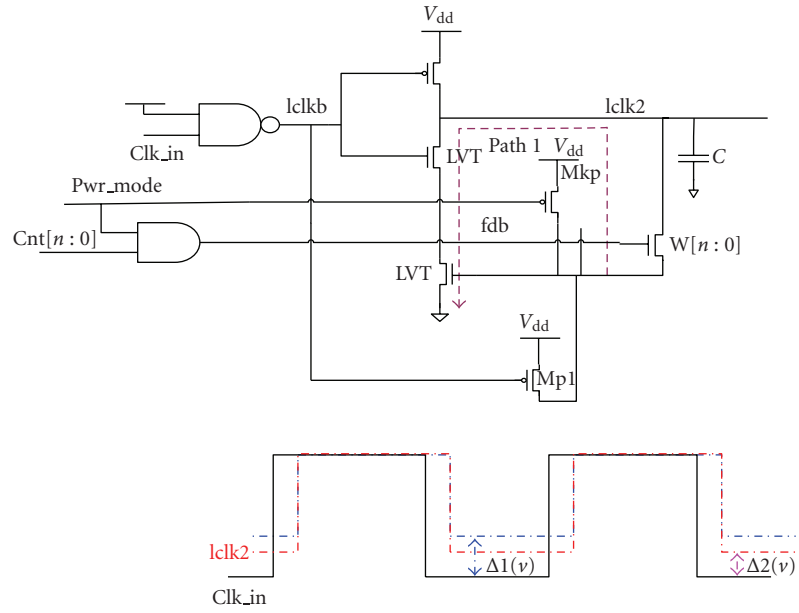

Figure 3: Programmable reduced voltage swing circuit and waveforms.

and vdd-vt where vt is the value of the threshold voltage of the LVT transistor. We developed another circuit (Figure 3) that gives programmability to the value to logic 0 based on control bits Cnt[n : 0]. The Programmable Reduced Voltage Swing (PRVS) circuit can vary the logic 0 value based on how many bits of Cnt[n : 0] bus are selected. Each of the Cnt[n : 0] bits corresponds to W[n : 0] transistor and it varies how fast the fdb node can be discharged to vt through the dotted path 1. Both Mp1 and Mkp are minimum size devices to pull up the fdb node and both have no impact on the circuit speed.

To summarize the differences of our proposed technique to traditional techniques in terms of some of the key design metrics we have the following.

(1) Area. Traditional LVS signaling requires an extra power supply routing of such an extra power supply network gives rise to considerable area overhead. RVS signaling does not require extra power supply and has only one extra transistor for each inverter.

(2) Power consumption. Active power consumption is proportional to signal voltage swing. As a result, LVS

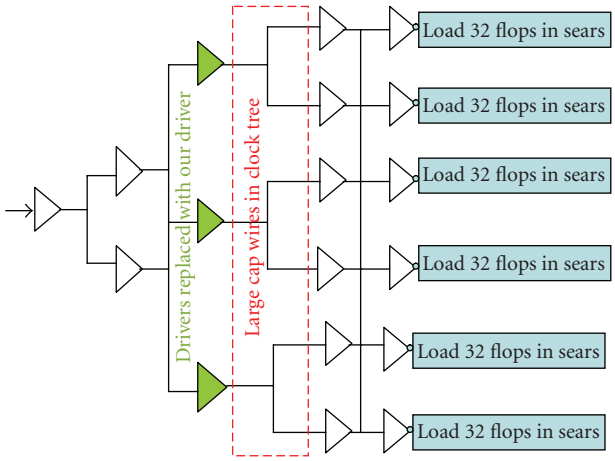

Figure 4: Spine and load circuit.

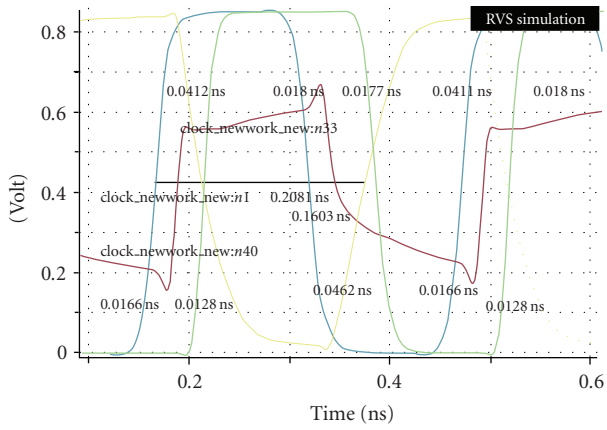

Figure 5: Output and RVS simulation waveform results.

and RVS signaling are equivalent in reducing signal voltage swing hence active power consumption.

(3) Performance. Low supply voltage and low logic 1 voltage in LVS signaling lead to performance degradation. While in RVS signaling, the constant supply voltage and logic 1 voltage do not degrade performance 2.

(4) Noise margin. The reduced signal voltage swing needs to cover the receiver flip-flop's meta-stability point (e.g., 0.5 V_{dd}), and the minimum distance from the metastability point to input signal voltage swing boundary gives noise

4. Simulation Result

We compared our proposed RVS inverter and traditional full voltage swing (FVS) inverter, we used HSPICE tools for the simulation, and results for the two inverters with 2.00 fF load capacitance under 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, and 1.5 V supply voltage are shown in Table 1. Table 1 gives the average comparison results between FVS and RVS inverters.

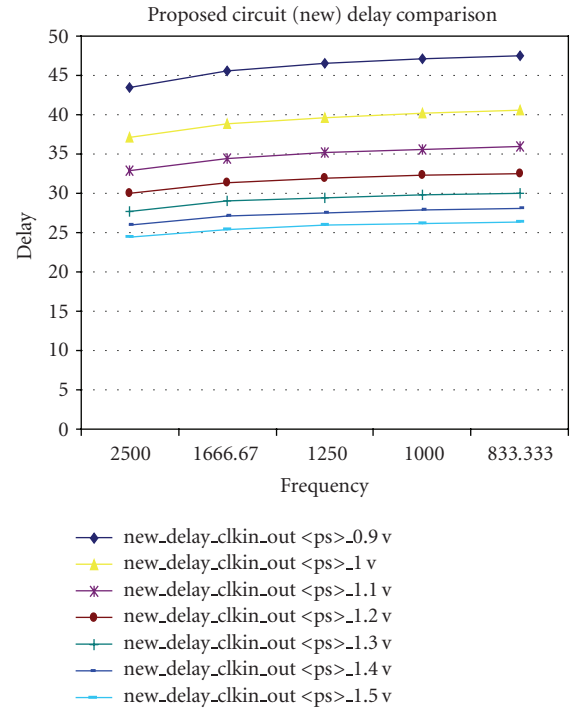

Figure 6: Proposed circuit delays with different voltages.

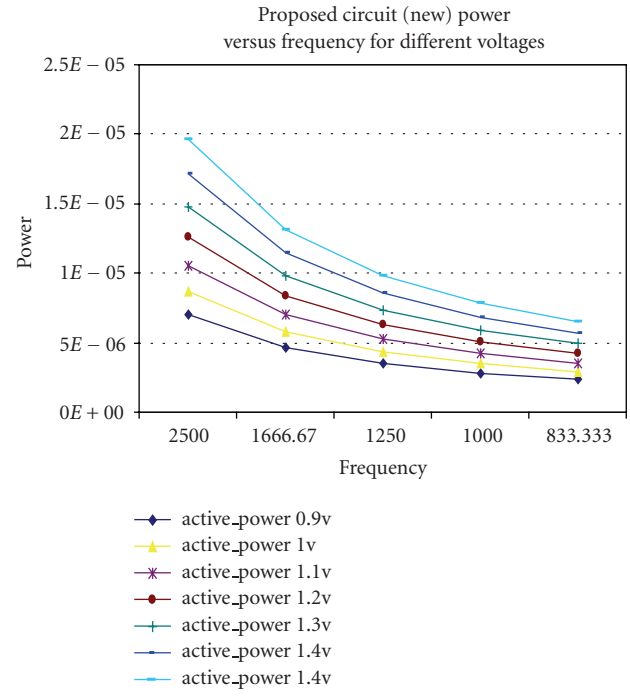

Figure 7: Proposed active power with different voltages/frequency.

To further verify this approach, we build a clock spine which drives an array of 6 × 32 = 192 flip-flops. HSPICE simulation shows that by replacing the clock buffers with the proposed RVS buffers as shown in Figure 4, we achieve 37.2% power reduction, while the signal propagation delay from the spine input to a flip-flop is degraded by 8.6%, and

clock signal slew rate is degraded by 30.0%. Table 2 gives the comparison results and Figure 5 shows waveform of RVS and output results.

We also verified the circuit still functioning with different voltages. Figures 6 and 7 show the results. Table 3 shows results with different cap, clock input pulse width, and different voltages.

5. Conclusion

In this paper, we propose Reduced-Voltage-Swing (RVS) signaling as compared to the traditional Low-Voltage-Swing (LVS) signaling for reduced active power consumption. We achieve minimum area overhead (without routing an extra power supply network and a minimum number of extra transistors), equivalent active power reduction, and minimum performance degradation. HSPICE simulation results using Arizona state university technologies with respect to a variety of design parameters (supply voltage, load capacitance, input signal slew rate, etc.) verify the effectiveness of these novel RVS circuits, which save an average of 37.2% dynamic power, with 8.6% clock insertion delay increase in a clock spine driving 192 flip-flops.

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