The High Power IGBT Current Source Inverter

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***Abstract*- This paper presents an investigation of the use of high voltage IGBTs in the Current Source Inverter (CSI) for high power motor drives. Modes are identified in the IGBT voltage waveforms which are discussed with respect to the IGBT ratings. This is followed by a detailed study of the switching transients within the CSI, particularly with regard to advanced gate drive techniques and snubberless operation. It will be shown that the conditions imposed on the IGBTs and diodes may be controlled and that snubbers are not necessary for voltage control.**

I. INTRODUCTION

The current source inverter is a popular choice for high power motor drives. The most common type of CSI is a load commutated thyristor bridge, although some IGCT based PWM drives have also been built. The GTO PWM CSI did not offer sufficient advantages over the thyristor version to make it popular. IGBTs rated at 4.5 kV and 1200A are available. With the advent of press pack devices [1], the IGBT is becoming an attractive alternative to the GTO and IGCT. The IGBT's gate drive requirements are modest, even for very high current devices. This advantage alone is significant where high reliability and a long service life are required. At these ratings, IGBTs are also alone in being able to current limit and voltage clamp for short periods. Another advantage is that IGBT switching transients may be shaped by a careful design of the gate drive [2].

The CSI has received little additional attention in the literature since the development of GTOs and PWM CSI methods. Adopting the IGBT as the switching device might be considered as straight forward, but the high voltage ratings of IGBTs come at some premium, in terms of both cost and losses, compared to the GTO and IGCT. Thus, to make a cost effective drive, careful consideration of the design of the CSI is required and advantage should be taken of the IGBT's features, rather than simply adopting it as a 'switch'. In particular it is important to quantify the voltage stress applied to the IGBTs and diodes to ensure that their ratings are not exceeded. In this paper, the circuit states are analyzed and it is shown that the device voltages may be defined and the effects of stray inductance are accounted for.

II. IGBT PWM CSI SWITCHING INTERVALS

In this work, the switching scheme applied is Space Vector Pulse Width Modulation (SVPWM). The advantages of this scheme over sinusoidal PWM were investigated by Espinoza et al. [3]. Typical SVPWM gating signals are shown in Fig. 1, with a carrier frequency (f_c) of 900 Hz, a fundamental output frequency (f_s) of 50 Hz, and Modulation Index (M) of 0.7. The carrier frequency in Fig. 1 is artificially low, to give a better view of the waveforms in the CSI. An overlap period of 1 μs is also included. These signals are applied to the gate drives of the three phase IGBT-based CSI; the IGBT currents take the same general form as the gating signals (apart from the overlap period), with an amplitude equal to that of the DC link current.

The phase shift in switching between the upper and lower switches, forming each inverter leg, is 180^0 and naturally there is 120^0 between any two upper or lower switches. Therefore, one cycle can be divided into six equal intervals each of 3.333 ms (60^0 as for the thyristor CSI). During three of the six intervals, any IGBT will have a 'fixed' state, either On or Off, while during its other three intervals the IGBT is subject to PWM switching. Also note in Fig. 1, all upper or lower IGBTs have PWM intervals, while one IGBT in the opposite set is 'fixed' On. Thus, there are three current paths

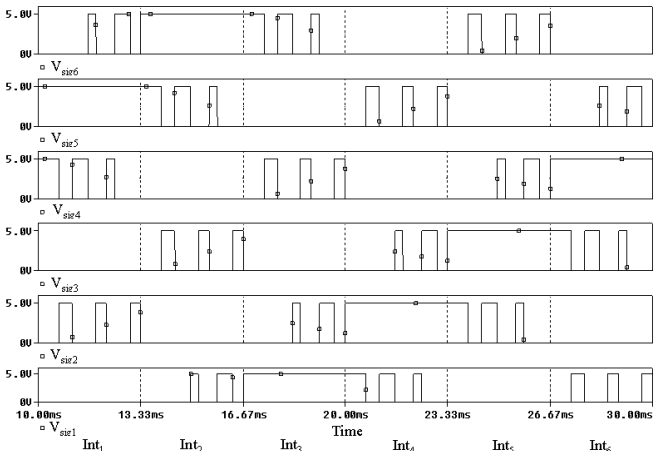

Fig. 1. SVPWM gating signals, V_{sig}1-6 applied to the gate drives of IGBTs 1-6, respectively

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during each interval. All nine possible current paths occur during one complete cycle. Six paths give non zero current vectors to the load while the other three paths give zero current vectors.

III. IGBT Voltage Modes

A switch 'Sw' (one IGBT and a series diode) is studied during each of the six inverter intervals, thus covering all aspects of the conditions applied to the IGBTs and diodes. Two modes may be seen in the voltage across a switch, when off, during its PWM interval. Each mode is defined by one or other of the remaining switches of the three under PWM switching.

For example, in the 3rd interval when $IGBT_4$ goes off, it is followed by $IGBT_6$, which in turn is followed by $IGBT_2$. Thus the voltage across $IGBT_4$ has two modes set by $IGBT_6$ and $IGBT_2$ in turn. However, at the end of the interval, the $IGBT_6$ pulse is dropped, so the first mode will not appear. This deviation from the classic SVPWM sequence is useful here to eliminate a short on-pulse of $IGBT_6$, which would be undesirable in a practical scheme. All possible current paths for the 3rd interval are indicated in Fig. 2. Two non zero states (a and c) and a zero state (b) are shown.

Thus the voltage (V_{sw4}) during the first mode is given by V_{ab} and during the second by V_{ac} (or $V_{ab}+V_{bc}$). Therefore, the polarity of V_{bc} during this interval (which is a load dependent) dictates the type of transition, whilst its value represents the step in the voltage across Sw_4. So, for positive V_{bc}, V_{sw4} increases to a higher voltage level, while a negative V_{bc} will cause V_{sw4} to fall to lower voltage level. This is a similar situation to the device voltages found in the simple thyristor converter. However here, in contrast to those, the frequency at which these voltages appear is the high carrier frequency, not a low multiple of the supply frequency or output frequency. The voltages V_{ab} and V_{ac} may take a range of values depending on the load conditions. Clearly negative voltages are blocked by the diodes, and these can also have the two modes during their blocking states.

IV. Controlled IGBT Switching In The CSI

Clearly, the situation may arise where the voltage in the first mode is blocked by the diode and in the second mode by the IGBT, with a high dv/dt occurring. This places stress on the IGBT and its gate drive; however, it is a similar situation to that encountered in voltage fed inverters at every switching instance. Therefore, a basic hard switched gate drive similar to that specified in the IGBT manufacturer's data sheet will be sufficient.

However, there is a trend towards using the IGBT's control over switching in various ways. This ability was demonstrated soon after the IGBT was first manufactured with the Active Snubber arrangement [4]. Active Voltage Control (AVC) has

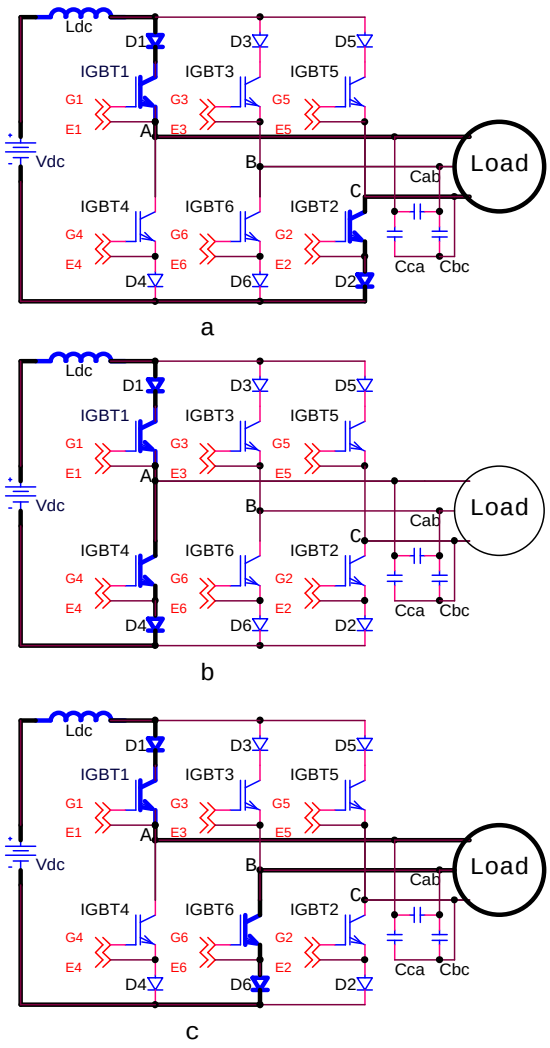

Fig. 2. The current paths during the on state of Sw_1 (during the 3rd interval)

also been proposed, particularly for IGBTs connected in series [5]. Over-voltage clamping, by means of zener diode feedback to the gate or other means, is also commonly considered [6]. As the AVC method offers most the features of the other methods, this type of control is considered here as representative. The main elements of the method are a collector voltage control loop, with a prescribed dv/dt during transitions, a limit voltage during the off period and saturation of the loop during the IGBT on period (to ensure low on-state losses).

All of these control methods require the IGBT to be in its active region to be able to control its behavior. Here, however, the IGBT is subject to rapid changes in collector-emitter voltage during its blocking state, when the modes are changing. Consequently, the usefulness of these advanced switching methods must be assessed.

V. Transition Between Modes

To define the voltage transients on switching, attention must be paid to the detail of the current commutation process. In the CSI, all switching instances require an overlap period between sequential IGBTs' gate pulses. This is necessary to ensure a continuous path for the DC link current. Current commutation occurs either at the beginning or at the end of the overlap period depending on the voltage polarity between the switching IGBTs. Considering the bottom switches in the inverter (Sw_2, Sw_4 and Sw_6), as before, a negative line voltage V_{bc}, for $IGBT_6$ followed by $IGBT_2$, causes commutation to occur at the beginning of the overlap period. In this case, the switch turning on, $IGBT_2$, controls the voltage transitions across the other switches as well as itself. The other switches have $IGBT_2$'s voltage plus an offset voltage given by the respective line voltage.

The diode in the switch conducting prior to commutation, D_6, will experience reverse recovery as it will block the negative voltage. This reverse recovery is controlled by any stray inductance in the loop (formed by the commutating switches and the output capacitor, Fig. 3) and by the voltage fall rate of the dominating switch.

On the other hand, in the case of a positive line voltage, as defined above, commutation occurs at the end of the overlap period under the control of the switch turning off, $IGBT_6$. During this commutation, the diode D_6 does not experience any reverse recovery as the current is forced to zero by $IGBT_6$ and there is no reverse voltage on the switch. Thus the diode's charge will be removed by recombination.

A similar argument can be made for the top switches in the inverter (Sw_1, Sw_3 and Sw_5), but with the position of commutation reversed for the same polarity of the line voltage.

Thus, depending on the line voltage polarity between the switching devices, the switches involved can be considered as master and slave. The master switch has a positive voltage during its off state, and therefore the IGBT characteristics are dominant. The master switch then dominates the current commutation and the voltage transitions during the overlap period. Conversely, the slave switch has a negative off state voltage and the diode's characteristics define its behavior. So at any switching instant, there is only one switch which dominates the commutation.

The equivalent circuit during commutation in a CSI can be simplified to a basic chopper circuit with an inductive load. The master switch is controlling, while the slave switch acts as the freewheeling diode. Thus the diode and IGBT behavior in the IGBT CSI is easily defined. The main voltage supported is given by the line voltages and the voltage overshoots determined by the stray inductance in the loop defined by the pair of devices commutating. The diode reverse recovery current depends on the stray inductance and the IGBT switching. This is explored for the chopper by Rahimo et al. [7].

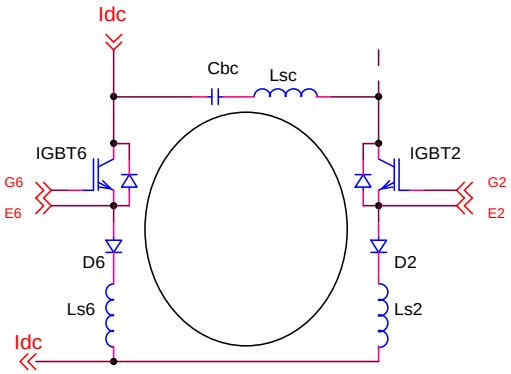

Fig. 3. Equivalent circuit and current loop during commutation between Sw_6 and Sw_2

VI. Simulation Results

The inverter shown in Fig. 2 was modeled in PSPICE. Fig. 4 shows the simulation results for the voltages V_{sw2}, V_{sw4} and V_{sw6} across the bottom switches Sw_2, Sw_4 and Sw_6, respectively. During each PWM interval, the two modes in the blocking voltage across each switch can be seen for both voltage polarities and a range of voltage magnitudes. The ac line voltage can be seen during the steady off-state intervals. Two ac line voltages can also been seen in the voltage modes during the PWM interval. The steady on-state interval rotates between switches.

A. *Active Voltage Control in a CSI*

Applying Active Voltage Control makes no significant difference to the waveforms of Fig. 4. Fig. 5 shows the gate-emitter voltage of $IGBT_4$ (V_{ge4}) and the scaled collector-emitter voltage of $IGBT_4$ (V_{fb4}), and similar waveforms for $IGBT_2$ and $IGBT_6$. The negative voltage excursions seen in Fig. 4 are removed by the series diode.

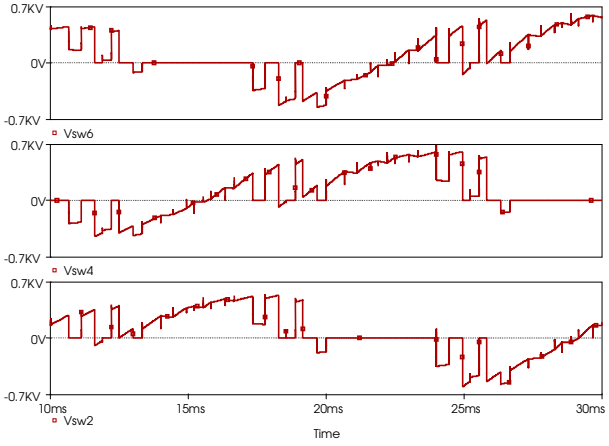

Fig. 4. Simulation results showing the voltage across the three bottom switches; V_{sw2}, V_{sw4} and V_{sw6}.

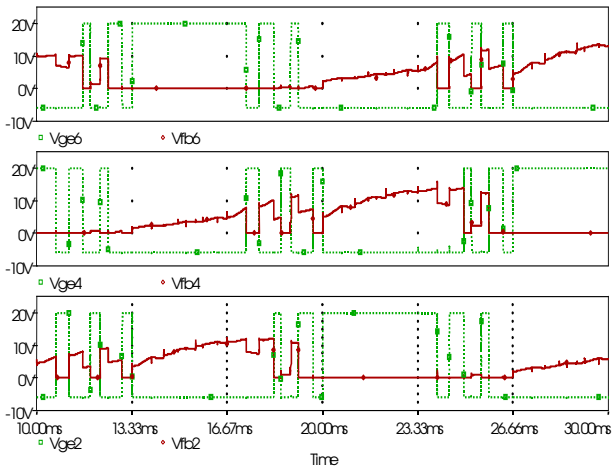

Fig. 5. Simulation results showing the gate-emitter voltage (V_{ge}) and the scaled collector-emitter voltage (V_{fb}) of IGBTs 2,4 and 6.

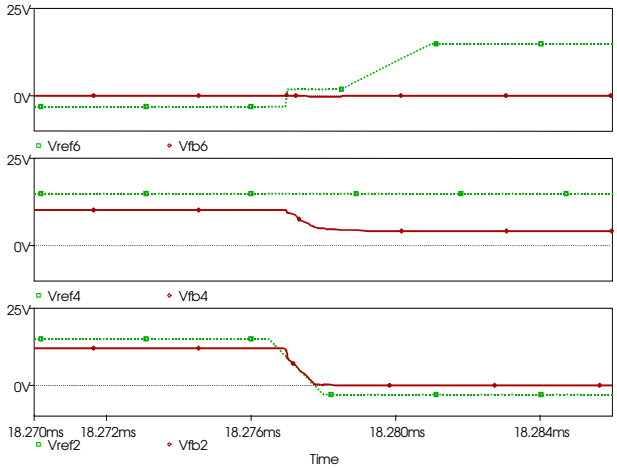

Fig. 7. The transition in V_{fb4} (scaled V_{ce4}) during its off state is controlled by Sw_2 as seen from V_{fb2} (scaled V_{ce2}).

The two modes in the off state voltage of each IGBT may be seen. Again, the voltage transition between these two modes can be either to a higher or a lower level depending on the line voltages.

As all the IGBTs in the CSI have similar voltage waveforms, with 120^0 phase shift, a detailed examination of a single IGBT will reveal all the important features. Fig. 6 shows the transition to a higher voltage level in V_{ce4} during its off state in the 5th interval. The transition occurs at the end of the overlap period. The shape of the transition is controlled by $IGBT_6$ under Active Voltage Control. The reference waveform for $IGBT_6$ is shown as well as the collector emitter voltage of $IGBT_6$. The reference voltage for $IGBT_4$ is seen to be high indicating that $IGBT_4$ is off. Similarly, $IGBT_2$ does not respond to its voltage reference as D_2 is blocking.

Fig. 7 shows the same traces as Fig. 6 for a transition in V_{ce4} to a lower voltage level (during the 3rd interval). Here, it is controlled by $IGBT_2$ which in its turn controls the rate of change of the diode's voltage in Sw_6 (not shown in the figure).

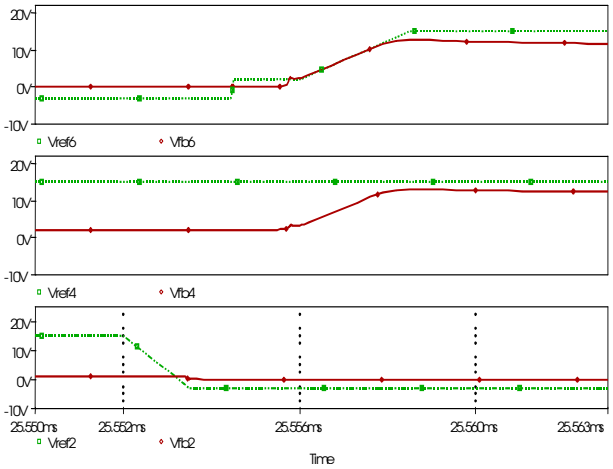

Fig. 6. The transition in V_{fb4} (scaled V_{ce4}) during the off state is controlled by Sw_6 as seen from scaled V_{ce6}.

B. *Active Snubber Technique in a CSI*

Similar results are obtained by applying the active snubber technique proposed in [4] to the CSI. The feedback resistor (R_f) used is 100 Ω and the feedback capacitor (C_f) is 3 nF. Fig. 8 shows a sample result indicating the control of an IGBT's voltage during the transition between modes by another IGBT. Sw_6 controls the rise in its voltage and that of V_{sw4}. Moreover, it controls the rise in the diode's voltage in Sw_2.

VII. Experimental Results

A scaled low power CSI was built using IGBTs with AVC. A PIC17C44 was used to generate the SVPWM. The

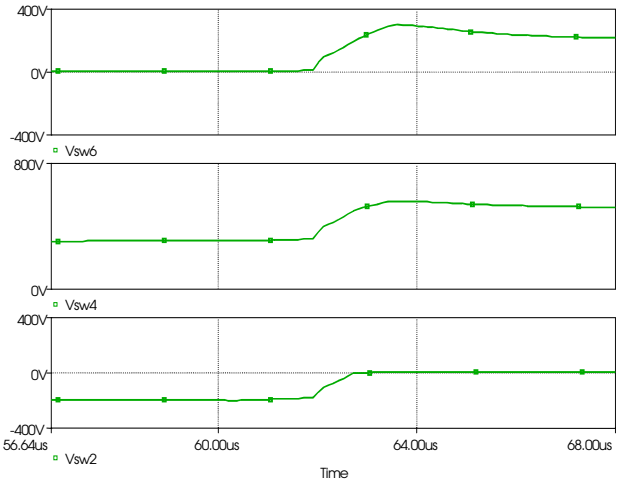

Fig. 8. The transition in V_{sw4} during the off state is controlled by Sw_6 which is actively snubbed.

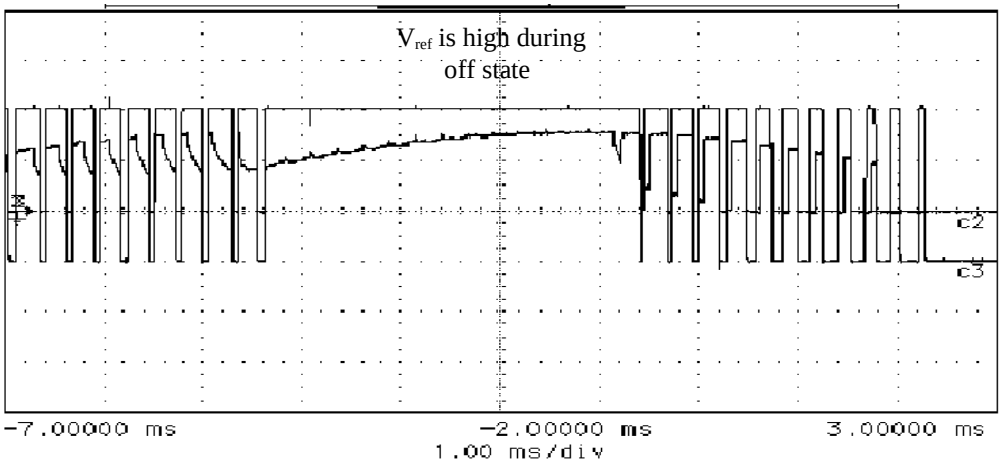

Fig. 9. C2: Scaled V_{ce} (V_{fb4}) and C3: reference signal (V_{ref4}) of one of the bottom switches (Sw_4) during half a cycle, showing the rise and fall in V_{fb4} within V_{ref4}.

switching frequency is 3.6 kHz. An overlap period of 800 ns was applied to the basic SVPWM signals and short pulses were also eliminated. A static inductive load was used (a three phase 2 kW induction motor with its rotor locked).

The experimental waveforms, Fig. 8, are pleasingly similar to those found by simulation (Fig. 4, Int_3, Int_4 and Int_5). It is clear that the $IGBT_4$'s voltage (V_{fb4}) has two modes during the PWM intervals of the reference signal (V_{ref4}) and the IGBT voltage is not under the direct control of the respective reference signal at all switching edges. During the steady off interval, the IGBT voltage is extremely smooth (a portion of the ac load voltage), illustrating the filter effect of the link inductor and the output capacitors.

Fig. 10 shows the experimental waveforms of the voltage across a switch; the gate-emitter voltage (V_{ge}), the switch voltage (V_{sw}), the collector-emitter voltage (V_{ce}) and the diode voltage (V_d). The waveforms are similar to that obtained by simulation in Figs. 4 and 5.

Fig. 11 shows the three phase load currents (i_a, i_b and i_c) which are nearly sinusoidal.

VIII. Discussion

Two modes have been identified in the voltages across the switches in the PWM CSI, variously seen in the figures above. From the consideration of these modes, it is clear that a conventional gate drive will be sufficient for the IGBT PWM CSI. The voltages occurring in each mode are defined by the line voltages at the inverter output. The master-slave concept identifies the circuit behavior by using a familiar chopper analogy. The master IGBT and slaving diode changes with the inverter state, as defined by the PWM. The output capacitors become the voltage source for the chopper analogy. Furthermore, the chopper analogy also accounts for the diode reverse recovery, including the effects of the stray inductances, and the IGBT switching behavior (for the master switch). Clearly, all the other voltages in the inverter are related to the master switch voltage, Figs. 6-8, with

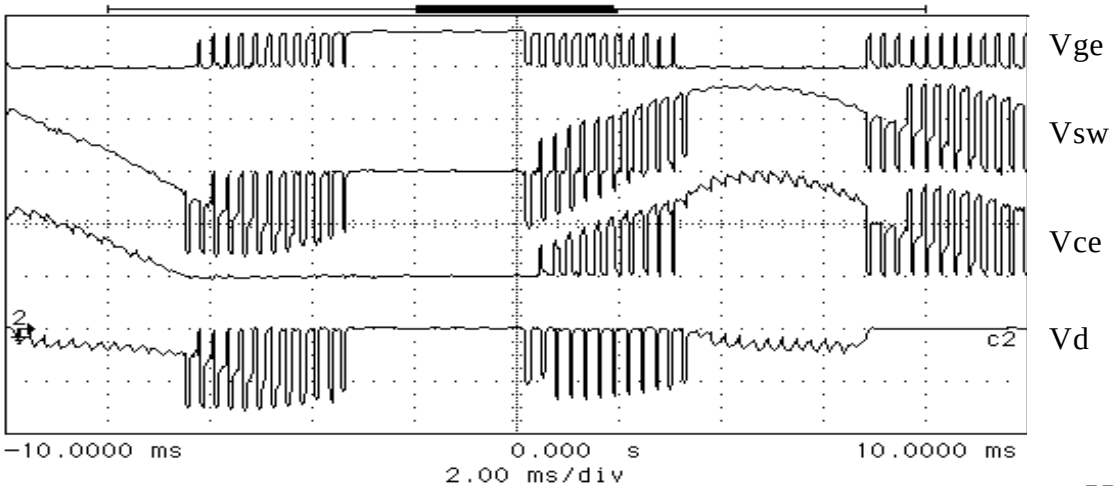

Fig. 10. Voltage waveforms across a switch in the CSI; gate-emitter voltage (V_{ge}), the switch voltage (V_{sw}), the collector-emitter voltage (V_{ce}) and the diode voltage (V_d)

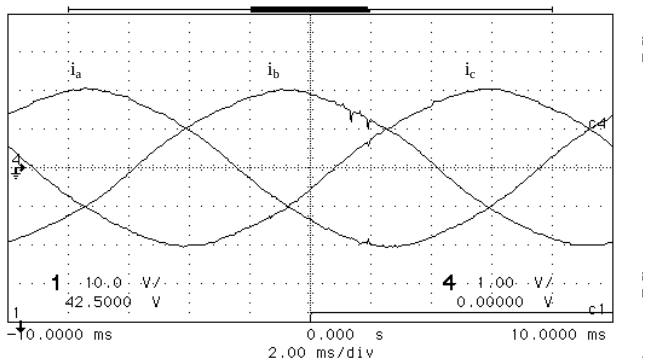

Fig. 11. The three phase output currents i_a, i_b and i_c (1A/div)

offsets due to the output capacitor voltages and voltages due to the stray inductance in the effective chopper circuit (included in the simulation and experiment).

Indeed, the voltage fall across an off switch is controlled by the falling voltage of the previous switch in the sequence (at the same inverter level). Similarly, the voltage rise is controlled by the rise of the voltage across the next switch in the sequence. As seen in Fig. 4, this argument is valid for both devices comprising the switch (the IGBT and the series diode). Table I summarizes how the transitions between voltage modes across a switch are controlled by the other switches. The transition type (increase or decrease) and thus the interval when it occurs, depends on the load power factor, as the phase in the output voltage changes with respect to the current.

Since all of the voltages are related to the master IGBT voltage, it follows that applying Active Voltage Control (AVC) to all IGBTs enables control of all the voltage transitions, whether by the AVC of the IGBT itself or by other IGBTs. The active snubber arrangement has the same effect. Both are attractive as they eliminate the need for passive snubbers controlling the dv/dt across the switches. Both approaches should take into consideration the maximum tolerable dv/dt of the IGBTs and their gate drives. The AVC can also be used to limit the IGBT peak voltage ensuring reliable operation under varying load conditions (over-voltage being signaled back to the PWM controller).

The use of AVC facilitates the use of IGBTs in series, as the conditions applied to the strings will be closely controlled. However, the voltage sharing in a string switch during its off state should be guaranteed by the addition of passive RC snubbers which is not intended to limit dv/dt [8].

The smooth voltage appearing at the output capacitors (and across the switches in some intervals) is one of the attractive features of the CSI. In large drives this is a well known advantage of the PWM CSI over the PWM VSI, where additional L-C filters are sometimes required and substantial DC link capacitors are employed.

IX. Conclusions

- There are two voltage modes across any off switch, depending on the PWM control.
- The transition between these two modes is under the control of the master switch.
- A set of mutual voltage control relationships between switches has been defined (Table I).
- Commutation occurs either at the beginning or at the end of the overlap period depending on the polarity of the line voltage between the commutating switches. The master switch is defined by this condition.
- The diode reverse recovery in a conducting switch is controlled by the turn on of the master switch in a basic chopper circuit.
- Passive snubbers to control dv/dts are not needed when the gate drive is designed for use in this circuit. Here, Active Voltage Control or Active Snubber methods were found appropriate.
- With Active Voltage Control, all voltage transitions are well defined, making the series operation of IGBTs in a CSI more feasible.

Acknowledgments

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TABLE I

Switches' Voltage (Vsw) Control During Transition Between Modes

Transition in Vsw	Voltage decrease during interval	Voltage decrease is controlled by Master Sw	Voltage increase during interval	Voltage increase is controlled by Master Sw
1	6	5	2	3
2	1	6	3	4
3	2	1	4	5
4	3	2	5	6
5	4	3	6	1
6	5	4	1	2

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