Commutation in a High Power IGBT Based Current Source Inverter

Muhammad Abu-Khaizaran and Patrick Palmer*
Faculty of Engineering, Birzeit University, Birzeit, P.O.Box 14, Palestine
email: mkhaizaran@birzeit.edu
*Department of Engineering, University of Cambridge, Cambridge, UK

***Abstract*— This paper presents an investigation of the effect of the commutation (overlap) period on the value of the output current and on the stability of a Current Source Inverter (CSI). The Current Source Inverter employs Insulated Gate Bipolar Transistors (IGBTs) as switches. A mathematical formula is developed to account for the overlap period and to explore the effects of various parameters on the deviation of the output current from the demand current. Also, this paper shows that the CSI during commutation is subject to oscillations due to diode reverse recovery and due to low output impedance of the "Master" switch. The effect of the commutation loop elements and the stray inductances are explored. The oscillations are shown in both simulation and experimental results. These oscillations necessitate the need for small RC snubbers, whose effect is also explored in analysis and experimentation. It will be shown that the snubbers not only dampen oscillations but they also achieve voltage sharing between series IGBTs or series diodes in the "Slave" or "Off" switches. The design guidelines for improving the performance of the CSI will be set.**

***Index Terms*— Current Source Inverter, Current Commutation, Space Vector Modulation, Series Operation, Voltage Sharing, Stability, Snubbers.**

I. Introduction

THE area of power inverters has rapidly grown over the past few decades with advances in devices, switching techniques and control strategies. The switching characteristics of the devices themselves, along with the development of switching methods, are now being exploited to improve the quality of the inverters, reducing their harmful effects on the utility grid, the load and the environment in general.

One of the most popular power inverters is the Voltage Source Inverter (VSI), which is widely used in motor drive applications. Thorough and intensive development has made the principles of its performance and operation very clear. On the other hand, the Current Source Inverter (CSI), despite its attractive features, has attracted very little attention, and its usage is rare. Until recently, it has been confined to high power drives that utilise Thyristors, GTOs or IGCTs [1], [2]. Recently, IGBTs of high power ratings have been developed, and are beginning to compete with the Thyristor based devices in high power applications. Being a voltage controlled device and being able to control its $\frac{dv}{dt}$ and $\frac{di}{dt}$ by its gate drive, and having fast switching features make the IGBT suitable for Pulse Width Modulation (PWM) operation. Consequently, the commutation circuits or the large snubbers are not needed in an IGBT based CSI, resulting in a high quality drive. This and other developments in devices make the CSI as attractive as the VSI. The rapid development in reverse blocking devices (GTOs [3], IGCTs [2], Symmetric Gate Commutated Thyristors (SGCTs) [4] and IGBTs [5]) may yet make the CSI a potential replacement for the VSI due to reduced conduction losses.

However, high voltage IGBTs are still slow, rare and expensive. A higher voltage switch, therefore, can be constructed by serially connecting IGBTs. Various methods have been proposed to improve voltage sharing and overcome differences between series IGBTs, and these methods vary in their sophistication and accuracy [6]–[11]. Amongst these is the Active Voltage Control (AVC), which can be easily implemented and can reproduce the behavior of most other schemes. The latter method employs a closed loop around the IGBT, where the collector-emitter voltage (V_{ce}) is intended to follow a predefined reference signal [11], [12].

This paper is focused on the study of a CSI employing series IGBTs and a Space Vector Modulation (SVM) switching scheme. AVC method is applied to the gate drive of the IGBTs. Very small RC snubbers (compared to IGCTs snubbers) will be used to dampen oscillations associated with the reverse recovery of the diodes in the Salve switches. A photograph of the experimental rig is shown in Fig. 1. Employing fast switching devices, such as IGBTs, in a CSI allows increasing the switching frequency of SVM scheme. Hence, the size of passive components in the CSI (the DC link inductor and input and output capacitors) can be significantly reduced.

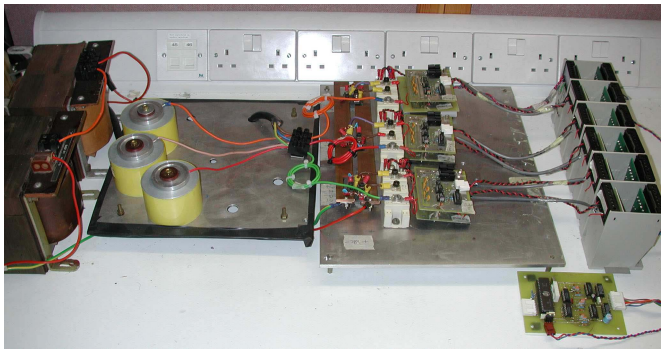


Fig. 1. A photograph of the experimental CSI setup

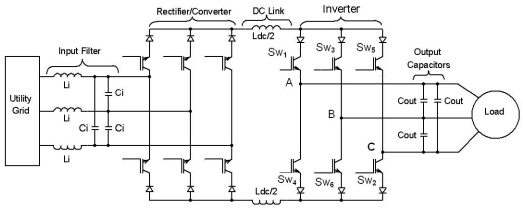


Fig. 2. A Modern Current Source Drive topology

II. Current Source Inverter Drive Topology and Space Vectors

A schematic of a modern Current Source drive is depicted in Fig. 2. It is composed of an input filter, a rectifier/converter, a DC link inductor, an inverter and output capacitors. Each switch in the CSI is composed of an IGBT and a series diode. Here, the CSI implements the Space Vector Modulation (SVM) as a switching scheme. SVM has several advantages over conventional sinusoidal PWM switching strategies, namely ease of generation and formation in digital circuits, also reduction of the switching frequencies for a similar harmonic content [13]. A typical set of SVM gating signals are shown in Fig. 3, with a carrier frequency (f_c) of 900Hz, a fundamental frequency (f_s) of 50Hz and a Modulation index (M) of 0.7. The carrier frequency was artificially low to produce reasonable pulse widths for both zero and non-zero states, and hence to give a better view of the waveforms under all conditions. The SVM signals were applied (after some modification) to the AVC gate drives of the IGBT based CSI that has the standard numbering sequence equivalent to the sequence shown in Fig. 2.

One cycle of each gating signal, 20ms in this case, can be divided into six equal intervals of 3.333ms (60°). During three intervals of a cycle, a particular IGBT has a fixed state, either on or off, whilst during the other three intervals, the IGBT is subject to PWM switching. The three IGBTs at the same level of the inverter (top or bottom) have their PWM intervals simultaneously, whilst there is only one IGBT in the opposite level conducting.

III. The Effect of Commutation (Overlap) Period on the Output Current

A. Mathematical Formula for the Output Current Deviation

In the CSI, a commutation (overlap) period is essential to ensure that there is no danger of there being no path for the DC link current, as this would lead to overvoltages. The overlap period must be long enough to turn on the off switch before turning off the conducting switch. The current commutation between any two switches depends on the polarity of the line voltage between the two commutating switches, and hence the switches' voltages [14]. The exact commutation instance occurs either at the beginning or at the end of the overlap period. However, ambiguity in the exact commutation instance implies a loss of control and uncertainty in the switch current, and subsequently the output line current during the overlap periods. Thus for this period, the magnitude of the output current is not under the direct control of the SVM scheme, but is controlled by the line voltages. To predict the deviation of the output current from the demand current reference (I_{ref}), define the output line current as:

$$I_l(t) = I_+(t) - I_-(t) \tag{1}$$

where $I_+(t)$ and $I_-(t)$ are the time functions of currents in the top and bottom switches of the same leg, respectively; their magnitudes equal I_{dc} during conduction. The output line current (I_l) is assumed to be positive when it is flowing out of the midpoint of the respective inverter leg.

Considering SVM, the sequence of the gating signals is 1, 3, 5, 1,... for the top switches and 2, 4, 6, 2,... for the bottom switches, with an overlap period added between any two subsequent gating signals. Fig. 4(a) through (c) shows the gating signals (V_{ge1}, V_{ge3} and V_{ge5}) with the overlap periods being shaded. Considering the 2^{nd} leg, the current deviation is governed by the polarity of V_{ba} at the rising edge of the gating signals (applied to the switches in the 2^{nd} leg) and by V_{bc} at the falling edge. A positive line voltage results in a decrease in the conduction period of the top switch and an increase in the conduction period of the bottom switch by the overlap period, and therefore (by applying (1)) in a decrease in the line current if it occurs during the positive half cycle of the line current and vice versa.

In Fig. 4, the shaded areas represent increases in the widths of gating pulses or current pulses due to the overlap period, whilst the dotted lines represent decreases in the widths of current pulses due to the overlap period. There are three possible deviations for a current pulse from its predefined

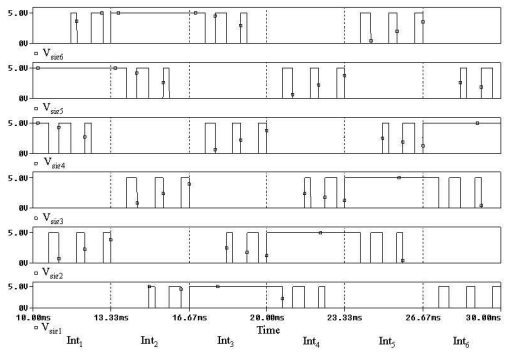


Fig. 3. SVM gating signals (V_{sig1},...,V_{sig6}) applied to the respective gate drives of the IGBTs

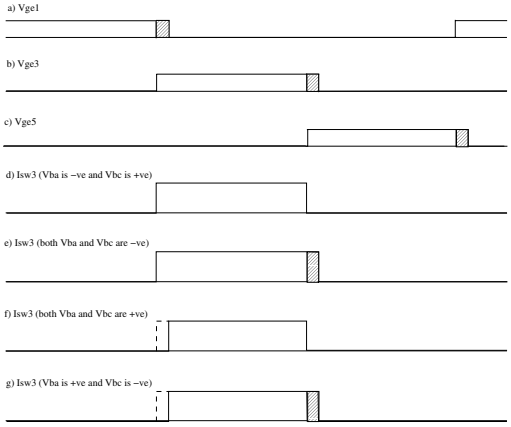


Fig. 4. The gating signals and I_{sw3} at different combinations of line voltages

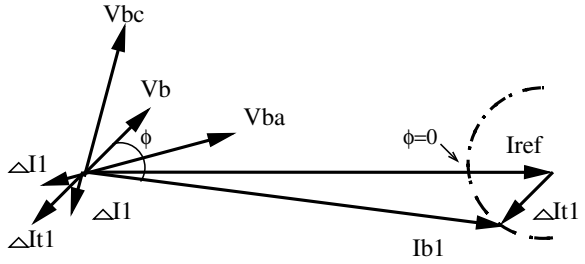


Fig. 5. The phasor representation of the fundamental voltages and currents with respect to the 2^{nd} leg

value. The current deviation can lengthen (Fig. 4(e)), shorten (Fig. 4(f)) or shift (Fig. 4(g)) the line current pulses by the length of the overlap period according to the output voltages. In the case of the specific combination of polarities of the line voltages, in Fig. 4(d) the overlap produces no current deviation.

Assuming ideal switches and nearly sinusoidal output voltages, the current deviation over one pulse edge (Δi) is:

$$\Delta i = T_o I_{dc} \tag{2}$$

The average current deviation (ΔI) over a half cycle and at one pulse edge is therefore:

$$\Delta I = \frac{(\frac{p}{2})\Delta i}{\frac{T}{2}} \tag{3}$$

where T_o is the length of the overlap period, p is the number of switching instances per one cycle ($p = \frac{f_c}{f_s}$), and T is the length of one cycle ($\frac{1}{f_s}$).

The deviation of the output line current from its reference is a square wave which is 180° out of phase with the respective line voltage. It, therefore, generates low order harmonics in the output and the DC link currents; these will be 5^{th}, 7^{th},... in the output and 6^{th}, 12^{th},... in the DC link [15]. These harmonics are hardly attenuated, because the DC link and output filters are usually designed for the high frequency harmonics related to the sidebands of the switching frequency. The phasor diagram of the fundamental components of the currents, the voltages and the current deviation related to the 2^{nd} leg is shown in Fig. 5. The subscript '1' denotes the fundamental components, and I_{b1} is the fundamental output line current of the 2^{nd} leg. The total current deviation (ΔI_t) is 180° out of phase with the phase voltage, and its value is given by:

$$\Delta I_t = \sqrt{3}\Delta I \tag{4}$$

The rms value of the fundamental component (ΔI_{t1}) of ΔI_t, which is a square wave, is given by:

$$\Delta I_{t1} = \frac{2\sqrt{2}}{\pi}\Delta I_t \tag{5}$$

Applying the cosine rule to the phasor diagram in Fig. 5, and simplifying yield a formula for I_{b1} as:

$$I_{b1} = -\Delta I_{t1} cos\phi + \sqrt{{I_{ref}}^2 - (\Delta I_{t1} sin\phi)^2} \tag{6}$$

Therefore, the per-unit value of I_{b1} ($I_{b1pu} = \frac{I_{b1}}{I_{ref}}$) is:

$$I_{b1pu} = -\delta I_{t1} cos\phi + \sqrt{1 - (\delta I_{t1} sin\phi)^2} \tag{7}$$

where δI_{t1} is the per-unit current deviation ($\delta I_{t1} = \frac{\Delta I_{t1}}{I_{ref}}$). δI_{t1} is inversely proportional to I_{ref}, which makes the current deviation more significant at low values of the output current. ϕ represents the displacement power factor angle. Equation (7) and Fig. 5 show that a unity displacement power factor yields a minimum value of the per-unit output current (I_{b1pu}). The rms value of the reference current in a CSI can be expressed as [13]:

$$I_{ref} = \frac{G_{ac} M I_{dc}}{\sqrt{2}} \tag{8}$$

where M is the Modulation index, and G_{ac} is the AC gain of the PWM scheme. By combining (2), (3), (4), (5) and (8), δI_{t1} can be expressed as:

$$\delta I_{t1} = \frac{4\sqrt{3}}{\pi}\frac{pT_o}{G_{ac}MT} \tag{9}$$

or

$$\delta I_{t1} = \frac{4\sqrt{3}}{\pi}\frac{f_c T_o}{G_{ac}M} \tag{10}$$

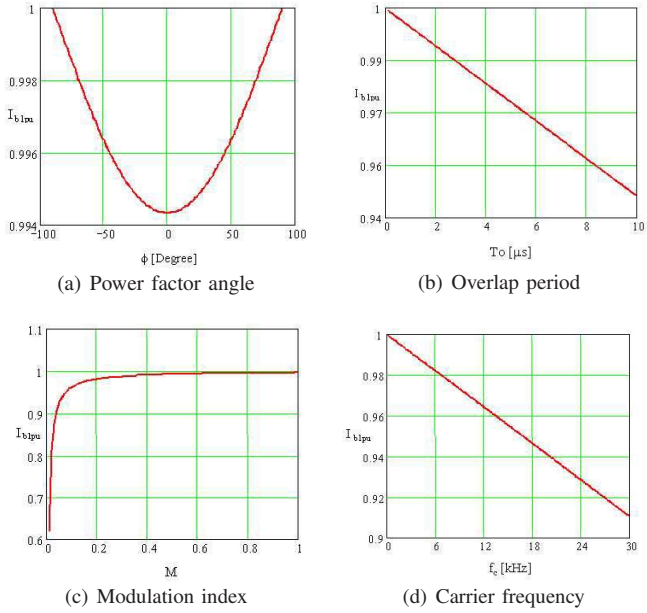
Therefore, the per-unit value of the fundamental current (I_{b1pu}) is:

$$I_{b1pu} = -\frac{4\sqrt{3} f_c T_o}{\pi G_{ac} M} cos\phi + \sqrt{1 - \left(\frac{4\sqrt{3} f_c T_o}{\pi G_{ac} M} sin\phi\right)^2} \tag{11}$$

Equation (10) represents the per-unit error in the output current that should be taken into consideration in case of open loop current or voltage control. Furthermore, not only is there a deviation in the current magnitude from the reference current, but the displacement power factor (pf) will vary from its predefined value as well, as can be seen from the phasor diagram of Fig. 5.

B. The Effect of Various Parameters on the Value of the Per-Unit Output Current

Equation (11) was implemented in MATHCAD to demonstrate the effect of various parameters on the per-unit current (I_{b1pu}). For SVM, the AC gain (G_{ac}) in (11) equals unity [13]. Fig. 6(a), (b), (c) and (d) shows the effects of ϕ, T_o, M and f_c, respectively, on the per-unit current. The default values used to generate these plots are: $T_o = 1\mu$s, $M = 0.7$, $f_c = 1.8$kHz and $\phi = 20^\circ$ (*i.e.* a displacement power factor of 0.94). Fig. 6(c) shows the serious effect of these parameters at light loads ($M < 0.1$), where the error can reach 35%; conversely the effect of ϕ on I_{b1pu} is tiny as seen in Fig. 6(a). Fig. 6(b) shows that the overlap period should be kept as short as possible to minimize the error in the per-unit current, but should be long enough to guarantee proper commutation. Also, Fig. 6(d) shows that the carrier (switching) frequency should be kept low to reduce the current deviation, which agrees with the minimized switching losses requirement, but contradicts with another requirement that the first significant harmonic being at a high frequency.



(a) Power factor angle (b) Overlap period

(c) Modulation index (d) Carrier frequency

Fig. 6. The effects of various CSI parameters on the per-unit current

IV. The Effect of Commutation Period on the Stability of the CSI

A. Master-Slave Combinations

In a CSI, current commutation occurs between switches at the same level of the inverter. Depending on the polarity of the line voltage between the commutating switches, the switches involved can be considered as a "Master" and a "Slave" [14]. A **Master switch** has a positive off-state voltage, and therefore the IGBT characteristics are dominant. The Master switch then dominates the current commutation and all voltage transitions during the overlap period. Conversely, the **Slave switch** has a negative off-state voltage and the diode characteristics define its behavior. The third switch at the same inverter level which is not involved in the commutation will be referred to as the **Off switch**. The voltages across the Slave and Off switches are therefore the Master switch voltage plus the respective line voltage. Hence, at any commutation instance, there is only one switch which dominates the commutation and voltage transitions: the Master switch. For example, the circuit during commutation between Sw_2 and Sw_4 is shown in Fig. 7.

B. Equivalent Circuits during Commutation

Considering the current commutation between the switches shown in Fig. 7, the voltage V_{ca} defines which switch is Master and which is Slave. Then the current commutation occurs either at the turn-on or the turn-off of the Master switch. Assuming that Sw_4 is initially off and turned on

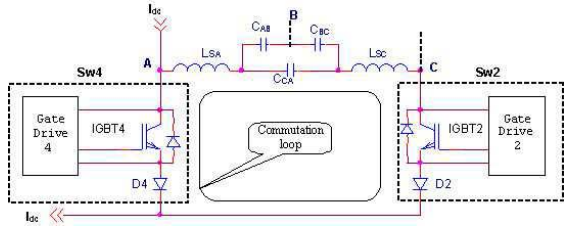
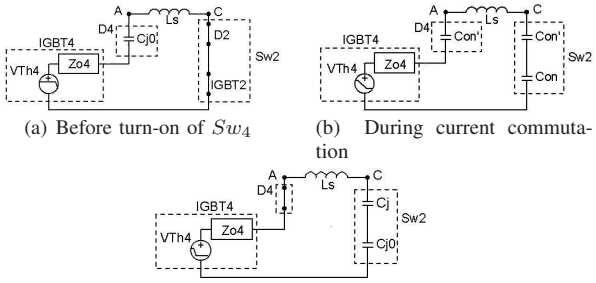


Fig. 7. The circuit during commutation between Sw_2 and Sw_4 in the CSI

at the beginning of the overlap period, whilst Sw_2 is still conducting and turned off at the end of the overlap period, the polarity of V_{ca} determines the instant of commutation. For example, if V_{ca} is negative, V_{sw4} is positive and $IGBT_4$ is blocking, and hence Sw_4 is the Master switch, whilst Sw_2 is the Slave. The current commutates from Sw_2 to Sw_4 immediately after turning on the Master (Sw_4); at the beginning of the overlap period. The fall in V_{sw4} is accompanied by a similar fall in V_{sw2} (causing a reverse voltage applied across the Slave (Sw_2)), both are controlled by Sw_4 (more precisely, by $IGBT_4$).

Three circuits can be derived for the current commutation, and these are shown in Fig. 8. The IGBT and its gate drive in the Master are represented by their equivalent Thévenin voltage source (V_{Th}) and output impedance (Z_o), whilst the other devices are represented by their equivalent capacitances. Circuits (a), (b) and (c) in the figure represent the effective circuit topology before, during and after the current commutation and the diode reverse recovery in the Slave switch (Sw_2). C_{j0} represents the diode junction capacitance at low voltages (zero bias), assuming the series diode and the anti-parallel diode of the IGBT are similar. C_j is the diode junction capacitance at a reverse voltage, $C_{on'}$ is the diodes capacitance during conduction, and C_{on} is the IGBT capacitance during on-state. L_s is the total stray inductance in the commutation loop including any added inductor, if there is any. The output capacitors of the inverter are assumed to have a negligible impedance during the commutation period (their capacitances are much larger than the devices' equivalent capacitances, therefore omitted from the circuit diagrams). The equivalent circuits regarding the Off-switch (Sw_6), which is not involved in the commutation, are treated separately, as they are connected in parallel with the equivalent circuits of the Slave switch (Sw_2) at point 'B' in Fig. 7. The equivalent commutation circuits at turn off of the Mater switch, or that include the Off switch may be deduced. However, the Master switch turn on is more crucial as it causes the reverse recovery of the diode in the Slave switch.

The different commutation instances in the CSI indicate the existence of an 'LC' circuit loading a voltage source, whose output impedance (Z_o) is very small at high frequencies [14]. Hence, voltage oscillations may occur at transitions as the damping of the loop is very small, as will be shown in the



(a) Before turn-on of Sw_4 (b) During current commutation

(c) After D_2's reverse recovery

Fig. 8. The equivalent circuits during the turn-on of the Master switch (Sw_4) and recovery of the diode in the Salve switch (Sw_2)

following subsection and in section VI. The damping of the loop can be increased by connecting an RC snubber across the diode capacitance (C_j) in the Slave switch [16]. C_j is very small compared to the other capacitances in the loop and has its maximum share of reverse recovery oscillations.

C. Simulation of Stray Inductance Effect on Reverse Recovery Oscillations

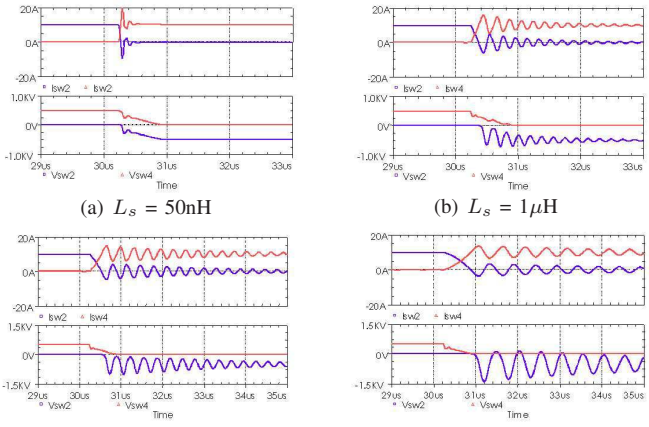
The simulation was carried out to explore the impact of the stray inductance (L_s) on the reverse recovery oscillations. The IGBTs in the simulation employ AVC method. Fig. 9 shows the voltages across the Master switch (V_{sw4}) and the voltage across the Slave switch (V_{sw2}) and their respective currents for various values of L_s. For large values of L_s, the AVC has a negligible effect on limiting the voltage across the diode in the Slave switch as seen in V_{sw2}. However, for $L_s \leq 3\mu$H, the Master switch tends to limit the reverse recovery oscillations. Hence, a small value of L_s is preferable.

V. Snubber Design

A. Resistor-Capacitor Snubber

The RC snubber has a double role in the CSI using series IGBTs; it increases the damping ratio of the 'LC' circuit which is loading the IGBT in the Master switch, and also it achieves dynamic voltage sharing in the controlled switches (the Slave or Off switches) during series operation [17].

The equivalent circuit shown in Fig. 10 models the commutation loop elements, the RC snubber and the parallel sharing resistor (R_p). The input voltage source represents the IGBT in the Master switch. The equivalent series resistance of all components in the commutation loop are lumped in r. Also, r accounts for the real part of the output impedance of the IGBT and its gate drive in the Master switch. The equivalent capacitances of the diode in the Master and Slave or Off switches are approximately dominated by the junction capacitance (C_j). The total stray inductance in the commutation loop is represented by L_s. R_s and C_s represent the proposed snubber. For the completeness of the snubber design, R_p is included in the model.



(a) L_s = 50nH (b) L_s = 1μH

(c) L_s = 3μH (d) L_s = 10μH

Fig. 9. The reverse recovery oscillations under AVC for four different values of stray inductance (L_s)

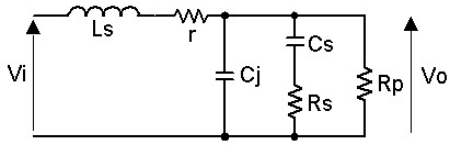


Fig. 10. Equivalent circuit during commutation including snubber

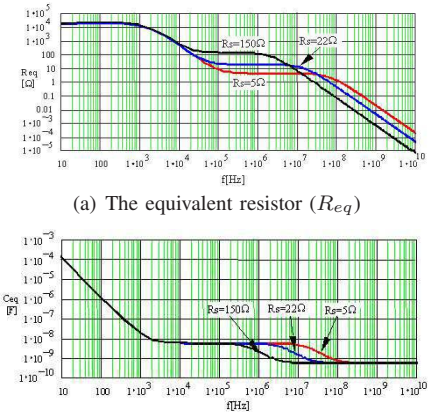
The effect of the snubber on the system response could be well understood if the equivalent impedance (Z_{eq}) of the parallel combinations (C_j//(R_s+C_s)//R_p) is found, which has the form:

$$Z_{eq} = \frac{R_p(1 + j\omega R_s C_s)}{(1 - \omega^2 C_s C_j R_s R_p) + j\omega(C_s(R_s + R_p) + C_j R_p)} \quad (12)$$

This impedance is composed of an equivalent resistor (R_{eq}) in series with an equivalent capacitor (C_{eq}), which are functions of the frequency (f). Consequently, the model in Fig. 10 behaves like a series RLC circuit, where $R = R_{eq} + r$ and $C = C_{eq}$.

The effect of the value of R_s on R_{eq} and C_{eq}, hence on the damping of the system, is shown in Fig. 11. The figure shows plots of R_{eq} and C_{eq} for L_s = 1μH, r = 0.05Ω, C_j = 500pF, C_s = 4.7nF, R_p = 20kΩ and different values of R_s. As R_s increases, the values of C_{eq} and R_{eq} start rolling off to their lowest values, at lower frequencies. This has two implications, the first is increasing the resonant frequency of the respective RLC, and hence reducing the rise time. The second implication is a reduced damping ratio at lower frequencies. However, very small value of R_s increases the initial discharging current of C_s, hence a reasonable small value of R_s should be used.

The choice of the snubber capacitor (C_s) is bounded by various constraints. The main purpose of adding C_s is to swamp the output capacitance of the off-device (IGBT or diode) so that the equivalent capacitance will be mainly dominated by the snubber capacitance. Subsequently, the voltage sharing, in the series string, during the transitions between different voltage levels will be dominated by the Master switch and the snubber capacitors. Choosing a large value of C_s, however, contradicts with other requirements,



(a) The equivalent resistor (R_{eq})

(b) The equivalent capacitor (C_{eq})

Fig. 11. The equivalent components of the snubber and the junction capacitance for R_s = 5Ω, 22Ω and 150Ω.

namely cost and power losses. Besides, large capacitors may result in unwanted attenuation of the high frequency components of the switching and slowing the response of the Slave or Off switches. Importantly, C_s should not affect the switching speed of the devices in the Master switch. Thus, a low value of C_s is essential.

It was found that for values of C_s close to C_j, the value of R_{eq} during the second plateau is much smaller than R_s and becomes closer to R_s as C_s was increased and approached 4.7nF (10 times C_j) [14]. Increasing C_s further, within the respective region, added a very little change in R_{eq}. Also, this change in C_s has a negligible effect on the roll-off frequency of both R_{eq} and C_{eq}. Therefore, a value of the snubber capacitance which is 10 times greater than C_j may be considered as the optimum value for C_s, which provides a compromise between the response time and the cost and power requirements.

B. Parallel Sharing Resistor

Parallel sharing resistor (R_p) is necessary to achieve static voltage sharing between series devices in an off switch. The value of R_p should be small compared to the other leakage resistors (of the off-IGBT or diode) to dominate the equivalent parallel resistor, and therefore to reduce the voltage sharing error between the series devices, which is dependent on the difference in leakage currents and output resistance, improving the voltage capability of each device. On the contrary, power losses requirements necessitate large values of R_p. A mathematical formula can be derived relating the power losses in the parallel resistors (P_{losses}), for two series devices, with the switch voltage (V_{sw}) and the difference in leakage currents (ΔI) as [14]:

$$P_{losses} = \frac{V_{sw}^2}{2R_p}\left(1+\left(\frac{R_p \Delta I}{V_{sw}}\right)^2\right) \qquad (13)$$

Fig. 12 shows a 3D plot of (13) for R_p between 1kΩ and 500kΩ, ΔI between 0 and 100mA, and V_{sw} of 2kV.

VI. Experimental Results of the CSI

In this section, the main issues regarding commutation and switching in a CSI, and in particular the use of the AVC technique, are addressed experimentally. The experimental rig was shown in Fig. 1. The IGBTs in the CSI employ SVM as a switching scheme and AVC as a seriesing method. The choice of the rig components is based on the simulation, with some amendment to certain values governed by equipment availability and suitability for work in the laboratory. The following subsections show various waveforms that validate the simulation and analysis conducted in this paper.

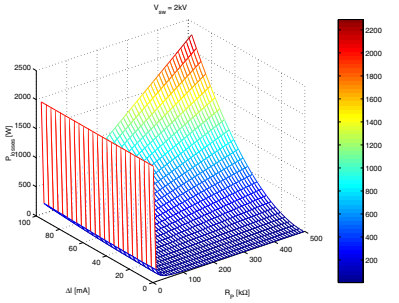


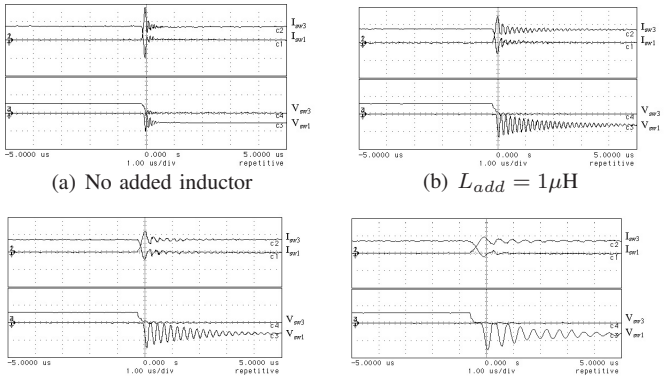
Fig. 12. A 3D plot of the power losses in the parallel resistors (P_{losses}) as a function of ΔI and R_p

A. Reverse Recovery Oscillations and Snubbers

Experiments were conducted on the CSI using four values of added inductance (L_{add}) in the commutation loop, emulating high power inverters and demonstrating the effect of loop inductance on CSI performance. Fig. 13 shows that the diode in the Slave switch (Sw_1) undergoes oscillatory reverse recovery at the turn-on of the Master switch (Sw_3). When an RC snubber of 39Ω and 4.7nF was connected across each diode, the reverse recovery oscillations have vanished as demonstrated in the figures of the following subsections.

B. Master-Slave Combinations

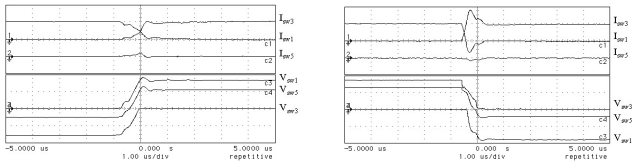
The three switches' voltages and currents during the turn-off and turn-on of the Master switch are shown in Fig. 14. In Fig. 14(a), Sw_1 is the Master switch, Sw_3 is the Slave switch, and Sw_5 is the Off-switch. V_{sw5} transits between two voltage modes, the second mode has a different voltage level and polarity from the first one. Clearly, all the voltage transitions have similar shapes apart from high frequency components being removed from V_{sw3} and V_{sw5}. The voltage overshoot across Sw_1 is imposed across Sw_5 as Sw_3 has started conduction. The figure also shows the charging current of Sw_5 which is needed to achieve its voltage transition. Two phases are seen in the current fall of I_{sw1} during turn-off. The first phase is attributed to charging the output capacitances of the Master, Slave and Off switches during the voltage rise. The current I_{sw1} falls to its tail value during the second phase after the voltage rise is completed. In contrast, Fig. 14(b) shows that the turn-on of the Master switch (Sw_3) controls the reverse recovery of the diode in the Slave switch (Sw_1), and also controls the transition in the voltage of the Off switch (Sw_5). The latter subfigure demonstrates the attractive feature of the AVC method in suppressing the voltage overshoot during the reverse recovery of the Slave switch which has diode characteristics.



(a) No added inductor (b) $L_{add} = 1\mu$H

(c) $L_{add} = 2.5\mu$H (d) $L_{add} = 9\mu$H

Fig. 13. The effect of added inductance on the reverse recovery oscillations in AVC. All voltages and currents are at 200V/div and 2.8A/div, respectively.



(a) Turn-off (b) Turn-on

Fig. 14. Voltages (200V/div) and currents (6A/div) in the three top switches at the turn-off and turn-on of the Master switch.

C. Series IGBTs in the CSI

Finally, the feasibility of using the AVC to implement series operation of IGBTs in CSIs is demonstrated experimentally. Sw_5 was constructed by connecting in series two identical IGBTs and a diode. An inductor of 1μH was inserted deliberately in the line to emulate high power inverters. An RC snubber of 10nF and 18Ω in parallel with a resistor (R_p) of 22kΩ was connected across each of these IGBTs. Fig. 15(a) shows the waveforms in the two series IGBTs during one cycle. The voltage sharing is good during both transient and steady state conditions. Fig. 15(b), on the other hand, was generated without the use of any type of snubbers across the series IGBTs. It shows that V_{ce5a} and V_{ce5b} differ despite using identical gate drives and IGBTs in the series string. During off-states, the gate drives of the respective IGBTs are inactive, but the dynamic voltage sharing is still assisted by the RC snubber, as shown in Fig. 16. Voltage sharing is achieved during both types of voltage transitions.

VII. Summary and Conclusions

The main conclusions from the analysis, simulation and experimental results can be summarized as:

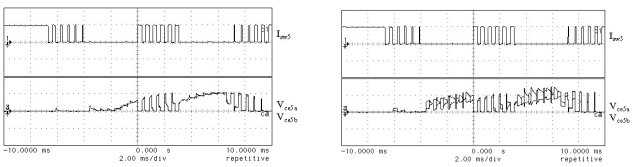
• A current deviation from the demand current is caused by the commutation in the CSI. Therefore, the overlap period should be accounted for especially in open loop current control.

• During any switching instance, there is only one switch (the Master switch) that controls the current commutation and the voltage transitions across itself and all other switches at the same inverter level (top or bottom).

• During reverse recovery, the junction capacitance of the diode in the Slave switch and the loop stray inductance behave like an LC circuit loading the Master switch. Therefore, the diode voltage may be susceptible to oscillations.

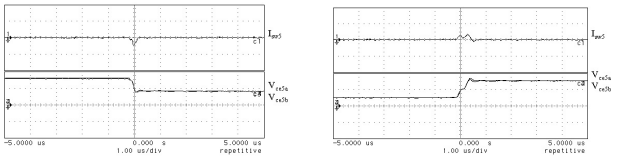
• A small RC snubber across each diode was found to be effective in suppressing the reverse recovery oscillations. Also, the AVC method was found to be effective in suppressing the voltage overshoot during diode reverse recovery.

• There is an important role of the RC snubber in achieving dynamic voltage sharing during the transition between voltage modes of an off-device, which is a feature of the CSIs. A large



(a) with snubbers (b) without snubbers

Fig. 15. One cycle of the voltage waveforms for two series IGBT employing AVC method. I_{sw5} (6A/div), V_{ce5a} and V_{ce5b} (150V/div).



(a) Voltage fall during an off-state (b) Voltage rise during an off-state

Fig. 16. The voltage sharing between two series IGBT in an Off-switch is achieved by RC snubbers. I_{sw5} (2A/div), V_{ce5a} and V_{ce5b} (100V/div).

parallel resistor (R_p) is necessary to achieve static voltage sharing during off-states.

• A compromise between the static voltage sharing error between the series devices and the power losses dictates the value of the parallel resistor (R_p).

References

[1] B. Wu and F.A. DeWinter. "Voltage Stress on Induction Motors in Medium Voltage (2300-6900V) PWM GTO CSI Drives". *IEEE Transactions on Power Electronics*, 12(2):213–220, March 1997.

[2] A. Weber, T. Dalibor, P. Kern, B. Oedegard, J. Waldmeyer, and E. Carroll. "Reverse Blocking IGCTs for Current Source Inverters". *PCIM'2000*, http://www.abbsem.com/data/nu00awa4.pdf, Nuremburg, June 2000.

[3] I. Omura and W. Fichtner. "Numerical Study of Reverse Blocking Switching Devices in Current Source Inverters, in Comparison with Normal Devices in Current Source Inverters and Voltage Source Inverters". *ISPSD'97*, pages 93–96, Weimar, Germany, May 1997.

[4] N.R. Zargari, S.C. Rizzo, Y. Xiao, H. Iwamoto, K. Satoh, and J.F. Donlon. "A New Current-Source Converter Using a Symmetric Gate-Commutated Thyristor (SGCT)". *IEEE Transactions on Industry Applications*, 37(3):896–903, May/June 2001.

[5] "IXRH50N120 Datasheet, IGBT with Reverse Blocking Capability". *http://www.ixys.com/l459.pdf*, IXYS Corporation, 3540 Bassett Street, Santa Clara, CA 95054, 2000.

[6] S. Hong, V. Chitta, and D.A. Torrey. "Series Connection of IGBTs with Active Voltage Balancing". *IEEE Transactions on Industry Applications*, 35(4):917–923, July/August 1999.

[7] G. Belverde, A. Galluzzo, M. Melito, S. Musumeci, and A. Raciti. "Snubberless Voltage Sharing of Series-Connected Insulated-Gate Devices by a Novel Gate Control Strategy". *IEEE Transactions on Power Electronics*, 16(1):132–141, January 2001.

[8] D. Zhou and D.H. Braun. "A Practical Series Connection Technique for Multiple IGBT Devices". *PESC'01*, 4:2151–2155, Vancouver, Canada, June 2001.

[9] K. Sasagawa, Y. Abe, and K. Matsuse. "Voltage Balancing Method for IGBTs Connected in Series". *IAS'02*, CD, Pittsburgh, Pennsylvania, October 2002.

[10] Y. Wang, A.T. Bryant, P.R. Palmer, S.J. Finney, M. Abu-Khaizaran, and G. Li. "An Analysis of High Power IGBT Switching under Cascade Active Voltage Control". *in Proc. IEEE IAS'05*, 2:806– 812, , Kowloon, Hong Kong, 2-6 October 2005. .

[11] A.N. Githiari, R.J. Leedham, and P.R. Palmer. "High Performance Gate Drives for Utilizing the IGBT in the Active Region". *PESC'96*, 2:1754–1759, Baveno, Italy, June 1996.

[12] P.R. Palmer and A.N. Githiari. "The Series Connection of IGBTs with Active Voltage Sharing". *IEEE Transactions on Power Electronics*, 12(4):637–644, July 1997.

[13] J.R. Espinoza and G. Joós. "Current-Source Converter On-Line Pattern Generator Switching Frequency Minimization". *IEEE Transactions on Industrial Electronics*, 44(2):198–206, April 1997.

[14] M.S. Abu-Khaizaran. *"The Design of a High Power IGBT Based Current Source Inverter Drive"*. PhD thesis, University of Cambridge, Cambridge, UK, January 2003.

[15] T. Halkosaari, K. Kuusela, and H. Tuusa. "Effect of Non-idealities on the Performance of the 3-phase Current Source PWM Converter". *PESC'01*, 2:654–659, Vancouver, Canada, June 2001.

[16] A.N. Githiari and P.R. Palmer. "Analysis of IGBT Modules Connected in Series". *IEE Proc.-Circuits Devices Syst.*, 145(5):354–360, October 1998.

[17] P.R. Palmer and M.S. Abu-Khaizaran. "The Series Connection of IGBTs in a Current Source Inverter". *PESC'01*, 1:170–175, Vancouver, Canada, June 2001.