A Single-Stage Zero-Voltage Zero-Current-Switched Full-Bridge DC Power Supply with Extended Load Power Range

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***Abstract*— A single-stage power-factor-corrected pulsewidth modulation converter with extended load power range is presented. The topology is based on a zero-voltage zero-current-switched full-bridge (ZVZCS-FB) inverter. Steady-state analysis of the topology shows that by operating the LC load filter in discontinuous mode, the dc-link voltage remains bounded and independent of the load level. Therefore, the load power range can be further expanded, including the no-load operating condition. The analysis also shows that the extension of the load power range is achieved without any penalty in: 1) the input power factor (due to the input current waveshaping feature); 2) the converter efficiency (due to ZVZCS and the single-stage features); and 3) the load voltage quality (due to the high bandwidth of the phase control loop). Simulated and experimental results are included to show the feasibility of the proposed scheme.**

***Index Terms*—Discontinuous operating mode, full bridge, high switching frequency, phase control, power factor correction, zero voltage zero current.**

I. Introduction

MOST electrical systems in the telecommunications field require high-power high-efficiency dc power supplies. The single-phase full-bridge (FB)-based topology has shown an excellent overall performance. This is due to its zero-voltage zero-current-switched (ZVZCS) operation—when it is phase-shift controlled—which provides near-zero switching losses. A high efficiency is, therefore, obtained. Moreover, in combination with a high switching frequency, high bandwidth and high power density can also be obtained [1]–[4].

Reference [5] has shown that by adding an auxiliary winding (Fig. 1): 1) the input current can be waveshaped and near unity input power factor is thus achieved and 2) the existing advantages of the ZVZCS-FB topology are preserved. Thus, the power supply is attained in a single stage, which allows an overall higher efficiency as compared to two-stage power supplies. However, the minimum load power is limited to 0.33 p.u. due to an excessive dc-link operating voltage below this limit.

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This paper proposes and demonstrates that, by operating the load LC filter in discontinuous mode, the low load power limit can be further reduced and, thereby, no-load operation is also allowed. The above feature is achieved without any penalty in the high performance of the power supply. Thus, the scheme presents high input power factor (>0.98), high efficiency (>85%), and extended load power range (from no load to full load).

II. Description of the Power Topology

A simplified scheme of the power supply is shown in Fig. 1. Simulated waveforms for a supply voltage $V_s = 220$ V and load power $P_l = 200$ W are shown in Figs. 2 and 3. To clearly show the waveshapes, a low switching frequency ($f_{sw} = 1.2$ kHz) was used. Proper design and control of the converter should assure a discontinuous input current (before filtering) to achieve a high power factor. This condition is obtained by forcing $N_{\rm aux} = N_{pri}$ (Fig. 1), and by properly selecting the auxiliary inductor $L_{\rm aux}$. The turns ratio of the transformer n_t is obtained by assuring the desired output voltage V_l for minimum supply voltage $V_{s\,\rm min}$. The value of the dc-link capacitor $C_{\rm dc}$ is obtained by limiting the maximum dc-link voltage ripple to a given value (e.g., $\Delta V_{\rm dc} < 2.5\%$). Finally, the second-order output filter $L_f C_f$ is calculated to operate the load inductor L_f in discontinuous mode and to limit the load voltage ripple to a given value (e.g., $\Delta V_l < 1\%$), both in the full-load power range.

A simplified analysis of the converter is done by considering that: 1) the dc-link capacitor $C_{\rm dc}$ and the load capacitor C_f are large enough to hold a constant dc-link voltage $V_{\rm dc}$ and load voltage V_l, respectively; 2) the diode D_{ch} conducts only during the startup of the power supply (it charges the dc-link capacitor $C_{\rm dc}$); and 3) all the components are ideal. The analysis is done breaking down the operation into four different modes.

Mode I, $(t_o - t_1)$ in Fig. 3(c): During this interval, there are two switches on in the inverter [either S_{g1} and S_{g3}, or S_{g2} and S_{g4}, Fig. 4(a)]. The switches remain on for a period given by $D/(2f_{sw})$. In this mode, energy from the dc-link capacitor $C_{\rm dc}$ flows to the output load R_l. Energy is also circulated from the ac mains into the loop formed by the switches S_{g1} and S_{g3} (or S_{g2} and S_{g4}), the primary and auxiliary windings of the transformer, one of the auxiliary diodes (either $D_{\rm aux1}$ or $D_{\rm aux2}$), the auxiliary inductor $L_{\rm aux}$, and a pair of diagonally

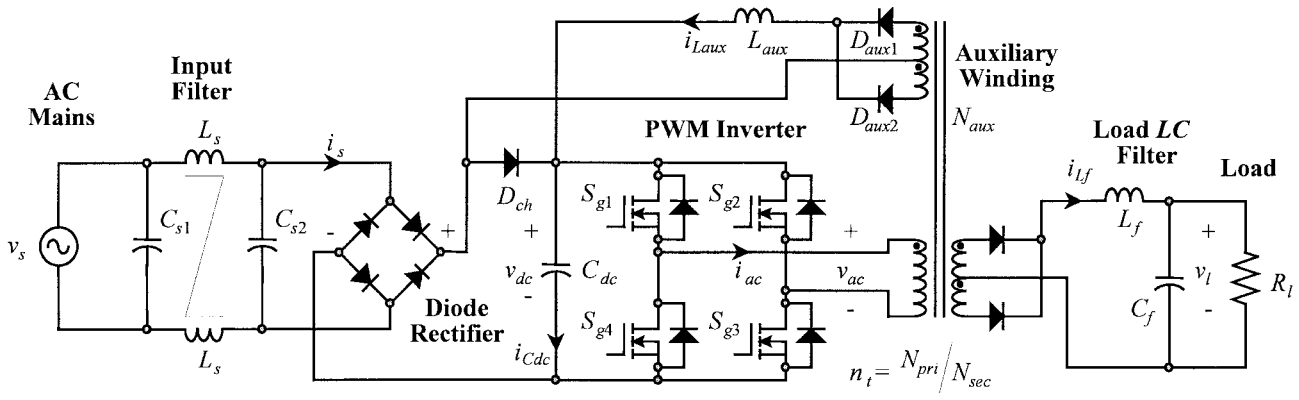


Fig. 1. Simplified scheme of the ZVZCS-FB power supply.

connected input rectifying diodes. Note that the thick lines in Fig. 4 represent the conducting closed loops.

Since $N_{\rm aux} = N_{pri}$, the auxiliary winding generates a voltage equal to $V_{\rm dc}$ that cancels the dc-link capacitor voltage. Thus, the voltage across the auxiliary inductor $L_{\rm aux}$ becomes only the rectified supply voltage $|v_s|$. This confirms that energy flows from the ac mains into the auxiliary inductor $L_{\rm aux}$ during this interval. Due to the high switching frequency, the supply voltage is assumed constant within an arbitrary interval k [Fig. 3(a)]. Therefore, the auxiliary inductor current expression in this mode becomes

$$i_{L_{\rm aux},k}(t) = \frac{|v_{s,k}|}{L_{\rm aux}}\, t \tag{1}$$

hence, at the end of the Mode I, the current in the auxiliary inductor $L_{\rm aux}$ in the interval k is found to be [Fig. 3(b)]

$$i_{L_{\rm aux},k\ \max} = \frac{|v_{s,k}|}{L_{\rm aux}} \frac{D}{2f_{sw}} \tag{2}$$

where $v_{s,k}$ is the average value of the supply voltage in the interval k, D is the duty cycle, and f_{sw} is the switching frequency. Note that proper design of the dc-link capacitor $C_{\rm dc}$ assures a near-constant dc-link voltage $V_{\rm dc}$; therefore, the steady-state duty cycle D remains constant, which results in a peak current in the auxiliary inductor (2) that depends only upon the supply voltage. Moreover, the peak current in the auxiliary inductor tracks the sinusoidal waveshape of the rectified supply voltage $|v_s|$ [Fig. 2(b)].

Similarly, if the load filter capacitor C_f is properly designed, the load voltage V_l is constant and, thus, the load filter inductor current expression becomes

$$i_{Lf}(t) = \frac{V_{\rm dc}/n_t - V_l}{L_f}\, t \tag{3}$$

hence, the load inductor current at the end of the Mode I is defined by [Fig. 3(d)]

$$i_{Lf\ \max} = \frac{V_{\rm dc}/n_t - V_l}{L_f} \frac{D}{2f_{sw}} \tag{4}$$

where $V_{\rm dc}$ is the average dc-link voltage and V_l is the average load voltage. Note that the peak load inductor current $i_{Lf\ \max}$ is independent of the interval k. This constant energy transferred to the load flows from the dc-link capacitor $C_{\rm dc}$ and becomes a constant negative peak current in the dc-link capacitor $i_{C\rm dc}$ [Figs. 2(e) and 3(e)].

Mode II, $(t_1 - t_2)$ in Fig. 3(c): In this mode, either the top switches S_{g1} and S_{g2} or the bottom switches S_{g3} and S_{g4} of the inverter remain on [Fig. 4(b)]. The energy stored in the auxiliary inductor $L_{\rm aux}$ during the previous mode is totally transferred into the dc-link capacitor $C_{\rm dc}$ as the auxiliary inductor current circulates through the dc-link capacitor ($i_{L_{\rm aux}} = i_{C\rm dc}$) in Mode II [Fig. 3(b) and (e)]. Since the stored energy in the auxiliary inductor $L_{\rm aux}$ depends upon the rectified supply voltage $|v_{s,k}|$, the positive peak current into the dc-link capacitor becomes time variant [Figs. 2(e) and 3(e)]. The voltage across the auxiliary inductor $L_{\rm aux}$ in Mode II is $|v_s| - V_{\rm dc}$, thus, the auxiliary current expression is as follows:

$$i_{L_{\rm aux},k}(t) = i_{L_{\rm aux},k\ \max} - \frac{V_{\rm dc} - |v_{s,k}|}{L_{\rm aux}}\, t. \tag{5}$$

This mode ends when the auxiliary inductor $i_{L_{\rm aux},k}$ current reaches zero. According to Fig. 3(b), this mode lasts $\Delta_{s,k}/(2f_{sw})$ and using (2), the following expression is found:

$$\Delta_{s,k} = \frac{|v_{s,k}|}{V_{\rm dc} - |v_{s,k}|}\, D \tag{6}$$

where $\Delta_{s,k}$ is the normalized period of Mode II. Equation (6) shows that the duration of this mode is time varying along one ac supply period. In order to assure a discontinuous input current, the normalized period $\Delta_{s,k}$ (6) must satisfy the expression $D+\Delta_{s,k} < 1$ at any interval k and load conditions. Using (6), this constraint can be written as

$$V_{\rm dc} > \frac{1}{1-D}\, |v_{s,k}|. \tag{7}$$

On the other hand, the load inductor current i_{Lf} freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_{\rm dc}$; therefore, the load inductor current is given by

$$i_{Lf}(t) = i_{Lf\ \max} - \frac{V_{\rm dc}}{L_f}\, t. \tag{8}$$

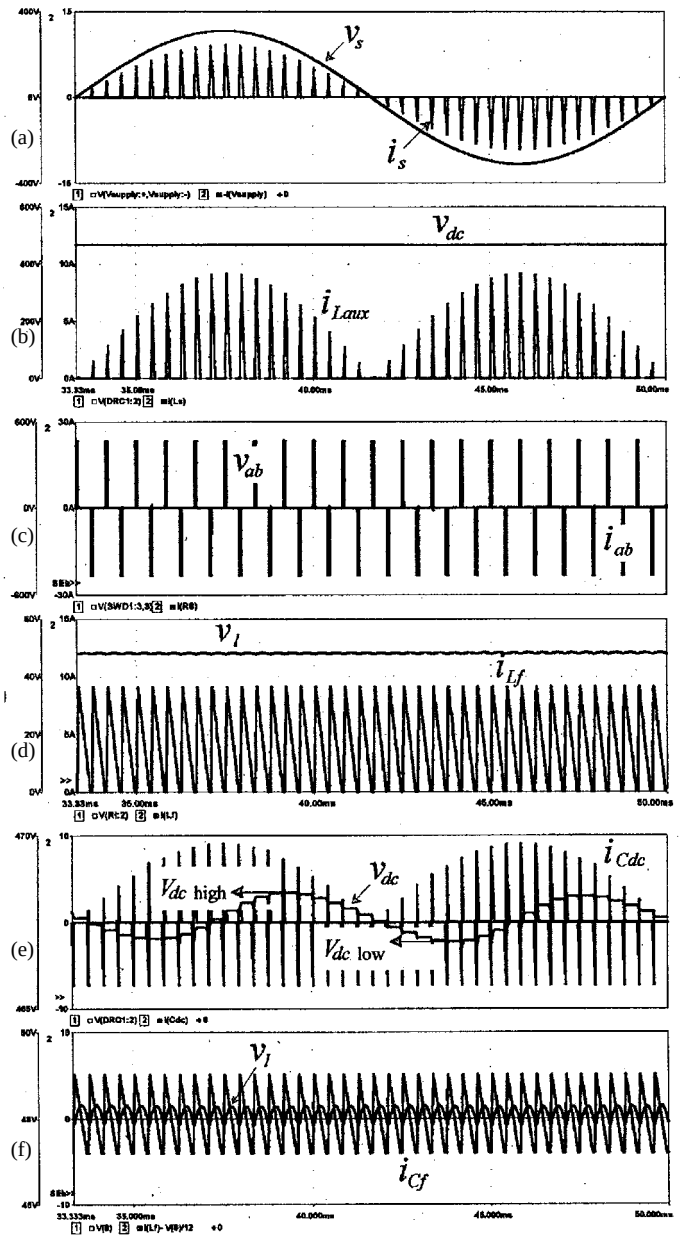


Fig. 2. Waveforms for the power supply shown in Fig 1. (a) Supply voltage (v_s) and current (i_s). (b) DC-link voltage ($v_{\rm dc}$) and auxiliary inductor current ($i_{L_{\rm aux}}$). (c) Transformer primary voltage ($v_{\rm ac}$) and current ($i_{\rm ac}$). (d) Load voltage (v_l) and load filter inductor current (i_{Lf}). (e) DC-link voltage ($v_{\rm dc}$) and dc-link capacitor current ($i_{C\,\rm dc}$). (f) Load voltage (v_l) and load capacitor current (i_{Cf}). $V_s = 220$ V and $P_l = 200$ W.

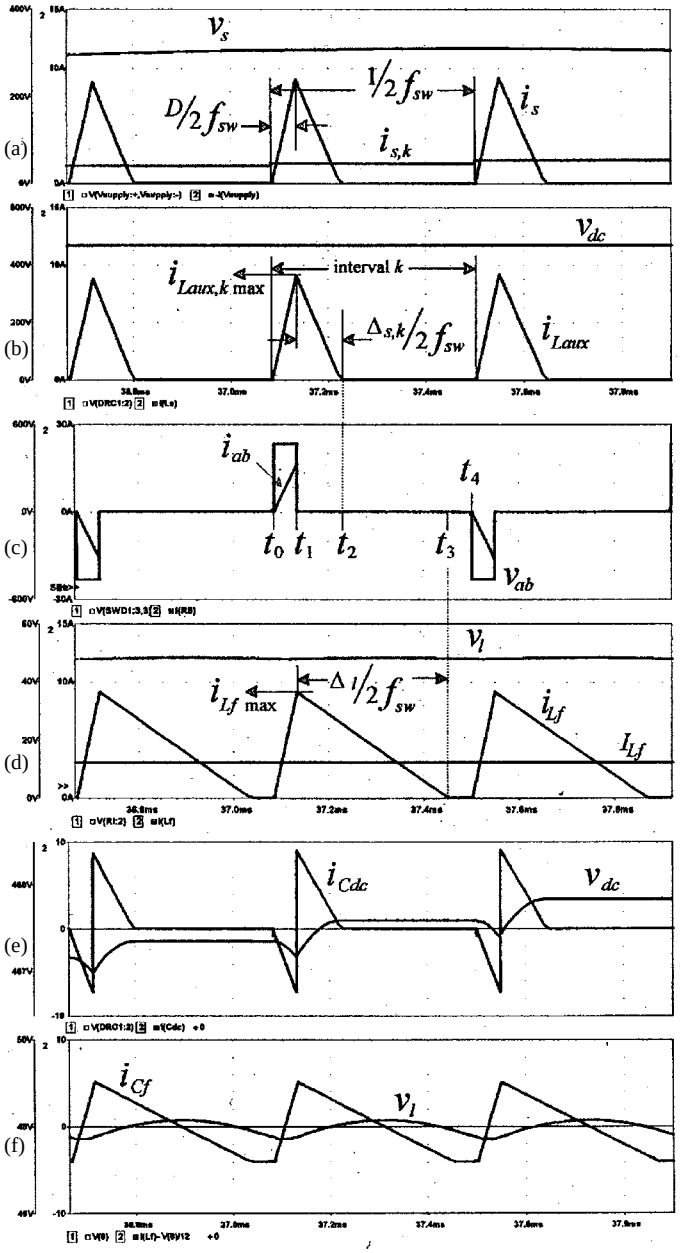


Fig. 3. Zoom-in of the waveforms shown in Fig. 2. (a) Supply voltage (v_s) and current (i_s). (b) DC-link voltage ($v_{\rm dc}$) and auxiliary inductor current ($i_{L_{\rm aux}}$). (c) Transformer primary voltage ($v_{\rm ac}$) and current ($i_{\rm ac}$). (d) Load voltage (v_l) and load filter inductor current (i_{Lf}). (e) DC-link voltage ($v_{\rm dc}$) and dc link capacitor current ($i_{C\,\rm dc}$), and (f) load voltage (v_l) and load capacitor current (i_{Cf}). $V_s = 220$ V and $P_l = 200$ W.

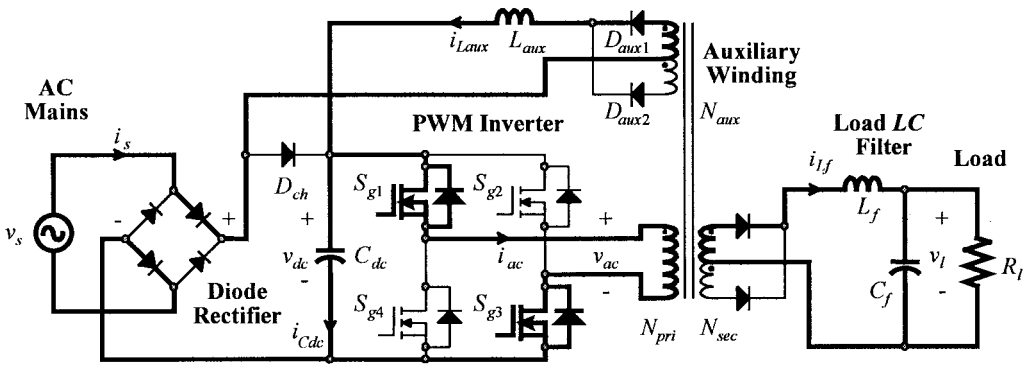
Mode III, $(t_2 - t_3)$ in Fig. 3(c): Like in the previous mode, either the top switches S_{g1} and S_{g2} or the bottom switches S_{g3} and S_{g4} of the inverter remain on [Fig. 4(c)]. This mode ends when the load inductor current i_{Lf} (8) reaches zero. According to Fig. 3(d), the load inductor current i_{Lf} decays for a period given by $\Delta_l/(2f_{sw})$ and using (4), the following expression is found:

$$\Delta_l = \frac{V_{\rm dc}/n_t - V_l}{V_l} D. \tag{9}$$

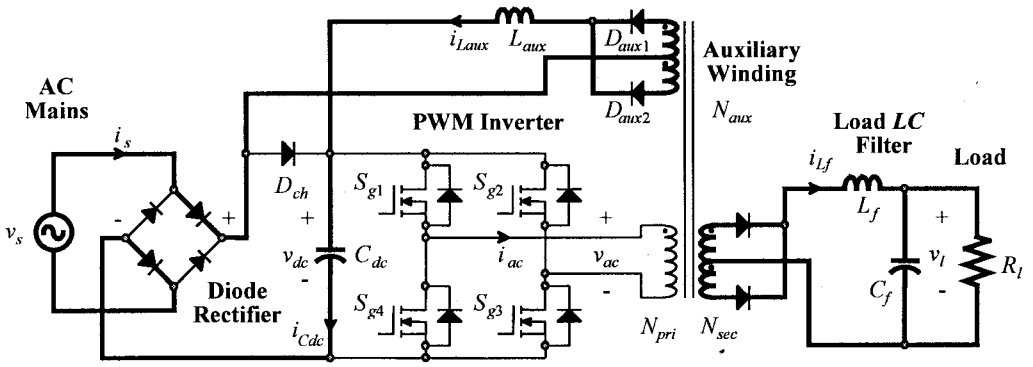
In order to assure a discontinuous load inductor current i_{Lf}, the normalized period Δ_l (9) must satisfy the expression $D + \Delta_l < 1$ at any load condition. Using (9), this constraint can be written as

$$n_t > \frac{V_{\rm dc}}{V_l} D. \tag{10}$$

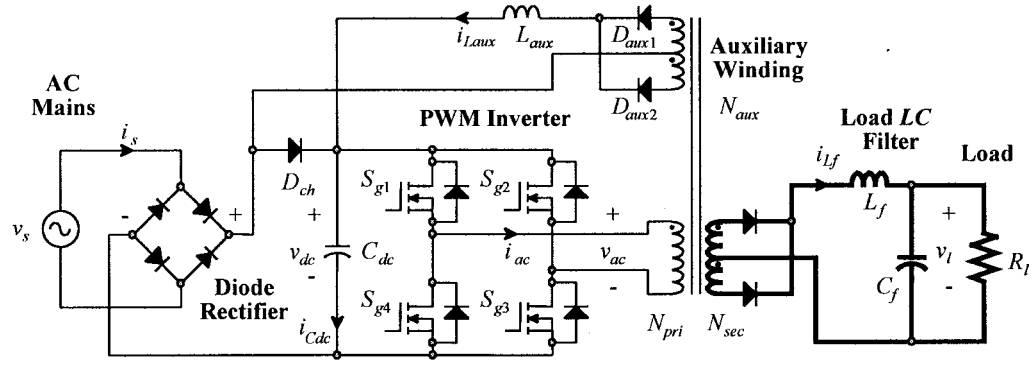
Mode IV, $(t_3 - t_4)$ in Fig. 3(c): Like in the previous mode, either the top switches S_{g1} and S_{g2} or the bottom switches S_{g3} and S_{g4} of the inverter remain on [Fig. 4(d)]. This mode ends when either the switches S_{g2} and S_{g4}, or S_{g1} and S_{g3}, are switched on and a symmetrical period begins. This mode lasts



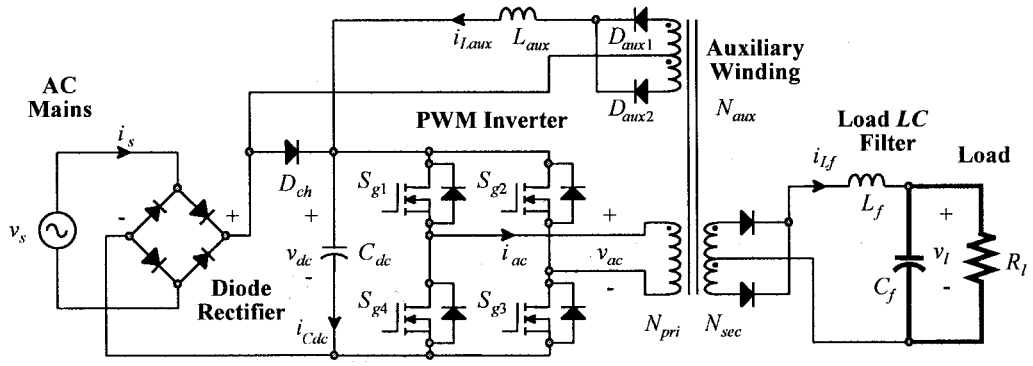
(a)



(b)



(c)



(d)

Fig. 4. Simplified scheme of the ZVZCS-FB converter. (a) Mode I [$t_o - t_1$ in Fig. 3(c)]. (b) Mode II [$t_1 - t_2$ in Fig. 3(c)]. (c) Mode III [$t_2 - t_3$ in Fig. 3(c)]. (d) Mode IV [$t_4 - t_5$ in Fig. 3(c)].

$1-D-\Delta_l$ [Fig. 3(d)]. Note that, in this mode. energy flows from the load filter capacitor C_f into the load R_l.

III. Design Equations

The proper operation of the power supply is assured by the appropriate selection of the transformer turns ratio n_t, the auxiliary inductor $L_{\rm aux}$, the dc-link capacitor $C_{\rm dc}$, and the load filter L_fC_f.

A. The Turns Ratio n_t of the Transformer

The load boundary condition $D+\Delta_l=1$ is obtained at minimum dc-link voltage $V_{\rm dc\ min}$, maximum duty cycle $D_{\rm max}$, and minimum supply voltage $V_{s\ \rm min}$. Note that, although the duty cycle D is constant within one ac mains period, it depends upon the supply voltage V_s and load power level P_l. Using (10), the load boundary condition can be expressed as

$$n_t=\frac{V_{\rm dc\ min}}{V_l}D_{\rm max}. \tag{11}$$

Using (7), the load boundary condition can also be expressed as

$$V_{\rm dc\ min}>\frac{1}{1-D_{\rm max}}\sqrt{2}V_{s\ \rm min} \tag{12}$$

where $V_{s\ \rm min}$ is the minimum rms supply voltage. Taking (12) at the limit, which is equivalent to considering the ac boundary condition ($D+\Delta_{s,\,k}=1$), in combination with (11), the turns ratio n_t of the transformer is

$$n_t=\frac{D_{\rm max}}{1-D_{\rm max}}\frac{\sqrt{2}V_{s\ \rm min}}{V_l}. \tag{13}$$

B. The Auxiliary Inductor $L_{\rm aux}$

The auxiliary inductor $L_{\rm aux}$ is calculated to supply the maximum load power $P_{l\ \rm max}$ at minimum supply voltage $V_{s\ \rm min}$. This condition is attained at maximum duty cycle $D_{\rm max}$. The average input power is

$$P_{su}=f_{su}\int_0^{1/f_{su}}v_si_s dt=\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}v_{s,\,k}i_{s,\,k} \tag{14}$$

where f_{su} is the ac mains frequency, f_{sn} is the normalized switching frequency ($f_{sn}=2f_{sw}/f_{su}$), and $i_{s,\,k}$ is the average input current in the interval k [Fig. 3(a)]. Using Fig. 3(a), $i_{L_{\rm aux}}=|i_s|$, and (6), the expression for $i_{s,\,k}$ is found to be

$$i_{s,\,k}=\frac{D^2}{4L_{\rm aux}f_{sw}}\frac{v_{s,\,k}}{1-|v_{s,\,k}|/V_{\rm dc}}. \tag{15}$$

If the converter is assumed lossless, the average input power P_{su} equals the load power P_l. Thus, using (14), (15), and maximum load power $P_{l\ \rm max}$ at minimum supply voltage $V_{s\ \rm min}$, the auxiliary inductor expression is found to be

$$L_{\rm aux}=\frac{D_{\rm max}^2V_{s\ \rm min}^2}{2f_{sw}P_{l\ \rm max}}\Psi_1 \tag{16}$$

where

$$\Psi_1=\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}\frac{\sin(2\pi k/f_{sn})^2}{1-(1-D_{\rm max})|\sin(2\pi k/f_{sn})|}. \tag{17}$$

The maximum duty cycle $D_{\rm max}$ is within the range $0.2<D_{\rm max}<0.8$ and the normalized switching frequency f_{sn} always satisfies $f_{sn}\gg 1$; therefore, (17) can be approximated by

$$\Psi_1\approx\frac{\pi/6}{0.1+D_{\rm max}} \tag{18}$$

thus, the auxiliary inductor expression (16) can be written as

$$L_{\rm aux}=\frac{D_{\rm max}^2V_{s\ \rm min}^2}{2f_{sw}P_{l\ \rm max}}\frac{\pi/6}{0.1+D_{\rm max}}. \tag{19}$$

C. The DC-Link Capacitor $C_{\rm dc}$

The average input power P_{su} over one ac mains period is equal to the load power P_l. However, the instantaneous input power waveform contains a large second harmonic, which, in turn, generates a second harmonic of voltage across the dc-link capacitor $C_{\rm dc}$. The dc-link capacitor is, therefore, designed to limit the second harmonic amplitude to a given small value and, thus, a constant duty cycle D operation is obtained. The maximum variation of energy in the ac mains is

$$\Delta E_s=\int_0^{1/4f_{su}}|v_si_s|\,dt=\frac{1}{2f_{sw}}\sum_{k=0}^{(f_{sn}-1)/4}|v_{s,\,k}i_{s,\,k}-P_l|. \tag{20}$$

The maximum dc-link voltage oscillation is found at maximum load power $P_{l\ \rm max}$ and minimum supply voltage $V_{s\ \rm min}$. This condition is attained at maximum duty cycle $D_{\rm max}$. Therefore, using (15), (19), and maximum load power $P_{l\ \rm max}$ at minimum supply voltage $V_{s\ \rm min}$, the expression for the maximum variation of energy in the ac mains (20) can be written as

$$\Delta E_{s\ \rm max}=\frac{D_{\rm max}^2V_{s\ \rm min}^2}{L_{\rm aux}f_{su}^2f_{sn}}\Psi_2 \tag{21}$$

where

$$\Psi_2\approx\frac{1}{f_{sn}}\sum_{k=0}^{(f_{sn}-1)/4}\cdot\left|\frac{\sin(2\pi k/f_{sn})^2}{1-(1-D_{\rm max})|\sin(2\pi k/f_{sn})|}\frac{\pi/6}{0.1+D_{\rm max}}\right|. \tag{22}$$

The maximum duty cycle $D_{\rm max}$ is within the range $0.2<D_{\rm max}<0.8$ and the normalized switching frequency f_{sn} always satisfies $f_{sn}\gg 1$; therefore, (22) can be approximated by

$$\Psi_2\approx\frac{3.66}{1+44.45D_{\rm max}} \tag{23}$$

thus, the expression for the maximum variation of energy at the ac mains side (21) is finally obtained as

$$\Delta E_{s\ \rm max}=\frac{D_{\rm max}^2V_{s\ \rm min}^2}{L_{\rm aux}f_{su}^2f_{sn}}\frac{3.66}{1+44.45D_{\rm max}}. \tag{24}$$

On the other hand, the maximum variation of energy in the dc-link capacitor $C_{\rm dc}$ can be expressed as

$$\Delta E_{\rm dc\ max}=\tfrac{1}{2}C_{\rm dc}V_{\rm dc\,high}^2-\tfrac{1}{2}C_{\rm dc}V_{\rm dc\,low}^2. \tag{25}$$

The maximum dc-link peak-to-peak voltage [Fig. 2(e)], which is obtained at minimum dc-link voltage $V_{\mathrm{dc\,min}}$, is given by $\Delta V_{\mathrm{dc\,max}} = V_{\mathrm{dc\,high}} - V_{\mathrm{dc\,low}}$ [Fig. 2(e)]. Therefore, using (12) at the limit, (25) can be written as

$$\Delta E_{\mathrm{dc\,max}} = C_{\mathrm{dc}} \frac{\sqrt{2} V_{s\,\mathrm{min}}}{1 - D_{\mathrm{max}}} \Delta V_{\mathrm{dc\,max}}. \tag{26}$$

Finally, if the converter is assumed lossless, then $\Delta E_{s\,\mathrm{max}} = \Delta E_{\mathrm{dc\,max}}$. Thus, using (24) and (26), the expression for the minimum dc-link capacitor C_{dc} is found to be

$$C_{\mathrm{dc}} = \frac{1}{\Delta V_{\mathrm{dc\,max}}} \frac{D_{\mathrm{max}}^2 V_{s\,\mathrm{min}}}{L_{\mathrm{aux}} f_{su}^2 f_{sn}} \frac{2.59(1 - D_{\mathrm{max}})}{1 + 44.45 D_{\mathrm{max}}}. \tag{27}$$

D. The Load Second-Order Filter $L_f C_f$

The load inductor L_f is calculated to assure a discontinuous operating mode under all load and ac mains conditions. The load capacitor C_f is designed to keep bounded the load voltage ripple. From Fig. 3(d), at the load boundary condition, $D + \Delta_l = 1$, it is found

$$I_{Lf} = \frac{V_l}{4 f_{sw} L_f} (1 - D) \tag{28}$$

where I_{Lf} is the inductor average current. From (28), the maximum load inductor L_f expression is found to be

$$L_f = \frac{V_l^2}{4 f_{sw} P_{l\,\mathrm{max}}} (1 - D_{\mathrm{max}}). \tag{29}$$

The maximum load voltage ripple $\Delta V_{l\,\mathrm{max}}$ occurs at maximum load power $P_{l\,\mathrm{max}}$ and maximum supply voltage $V_{s\,\mathrm{max}}$. In order to simplify the analysis, a maximum load voltage ripple $\Delta V_{l'\,\mathrm{max}}$, which is achieved at maximum load power $P_{l\,\mathrm{max}}$ and minimum supply voltage $V_{s\,\mathrm{min}}$, is introduced. This last condition is attained in continuous mode and, therefore, the following expression is valid:

$$\Delta V'_{l\,\mathrm{max}} = \frac{V_l}{32 f_{sw}^2 L_f C_f} (1 - D_{\mathrm{max}}). \tag{30}$$

From (30) and (29), the minimum load capacitor C_f expression is given by

$$C_f = \frac{P_{l\,\mathrm{max}}}{8 f_{sw} V_1 \Delta V'_{l\,\mathrm{max}}}. \tag{31}$$

IV. The Operating Region of the Power Supply

In this paper, the operating region is associated with the value of the dc-link voltage V_{dc} as a function of the load power P_l and supply voltage V_s obtained in steady state. In order to evaluate it, a case study is analyzed for both continuous and discontinuous load inductor current operating modes. The conditions are as follows: $V_l = 48$ V, $V_{s\,\mathrm{min}} = 85$, $V_{s\,\mathrm{max}} = 265$ V, $P_{l\,\mathrm{min}} = 25$ W, and $P_{l\,\mathrm{max}} = 250$ W. A low switching frequency ($f_{sw} = 1.2$ kHz) is used to clearly illustrate the waveforms. The component values have been calculated following the design criteria given in Section III. The values are shown in Table I.

TABLE I
Parameters Used in Figs. 2, 3, 5, and 6. *: Proposed Operating Mode

supply voltage range	$V_s = 85 \sim 265$ V	
supply frequency	$f_{su} = 60$ Hz	
load power range	$P_l = 25 \sim 250$ W	
load voltage	$V_l = 48$ V	
switching frequency	$f_{sw} = 1.2$ kHz	
max. duty cycle	$D_{\mathrm{max}} = 0.334$ (Fig. 7)	
turns ratio	$n_t = 1.256$ (13)	
auxiliary inductor	$L_{aux} = 1.62$ mH (19)	
dc link capacitor	$C_{dc} = 880$ µF (27)	
	Case A	**Case B***
LC inductor	$L_f = 18.3$ mH	$L_f = 1.28$ mH (29)
LC capacitor	$C_f = 120$ µF	$C_f = 1120$ µF (31)

A. The DC-Link Voltage V_{dc} Range

The dc-link capacitor C_{dc} is designed to limit the dc-link voltage ripple to a given value for both continuous and discontinuous load inductor current. Thus, the average supply current in an arbitrary interval k can be expressed by (15) regardless of the load inductor current mode. Therefore, the generalized average input power expression (14) using (15) can be expressed as

$$P_{su} = \frac{D^2}{4 L_{\mathrm{aux}} f_{sw}} \sqrt{2} V_s V_{\mathrm{dc}} \Psi_3 \tag{32}$$

where

$$\Psi_3 = \frac{\sqrt{2} V_s}{V_{\mathrm{dc}}} \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{\sin(2\pi k / f_{sn})^2}{1 - \sqrt{2} V_s / V_{\mathrm{dc}} |\sin(2\pi k / f_{sn})|}. \tag{33}$$

The dc-link voltage V_{dc} is always greater than the peak supply voltage and the normalized switching frequency f_{sn} always satisfies $f_{sn} \gg 1$; therefore, (33) can be approximated in the range $0 \le \sqrt{2} V_s / V_{\mathrm{dc}} \le 0.8$ by

$$\Psi_3 \approx \frac{0.48 \sqrt{2} V_s / V_{\mathrm{dc}}}{1 - 0.91 \sqrt{2} V_s / V_{\mathrm{dc}}}. \tag{34}$$

In continuous mode, the duty cycle D satisfies

$$D = \frac{V_l}{V_{\mathrm{dc}}} n_t. \tag{35}$$

Replacing the duty cycle expression (35) into the supply average expression (32) yields

$$P_{su} = \frac{1}{4 L_{\mathrm{aux}} f_{sw} n_t^2} \frac{\sqrt{2} V_s V_l^2}{V_{\mathrm{dc}}} \frac{0.48 \sqrt{2} V_s / V_{\mathrm{dc}}}{1 - 0.91 \sqrt{2} V_s / V_{\mathrm{dc}}}. \tag{36}$$

If the converter is considered lossless, (36) shows that, for a given supply voltage V_s, the dc-link voltage V_{dc} depends upon the load power level $P_l = P_{su}$. The values of V_{dc} that satisfy (36) are plotted in Fig. 5(a). They correspond to the operating region of the power supply in continuous mode. On the other

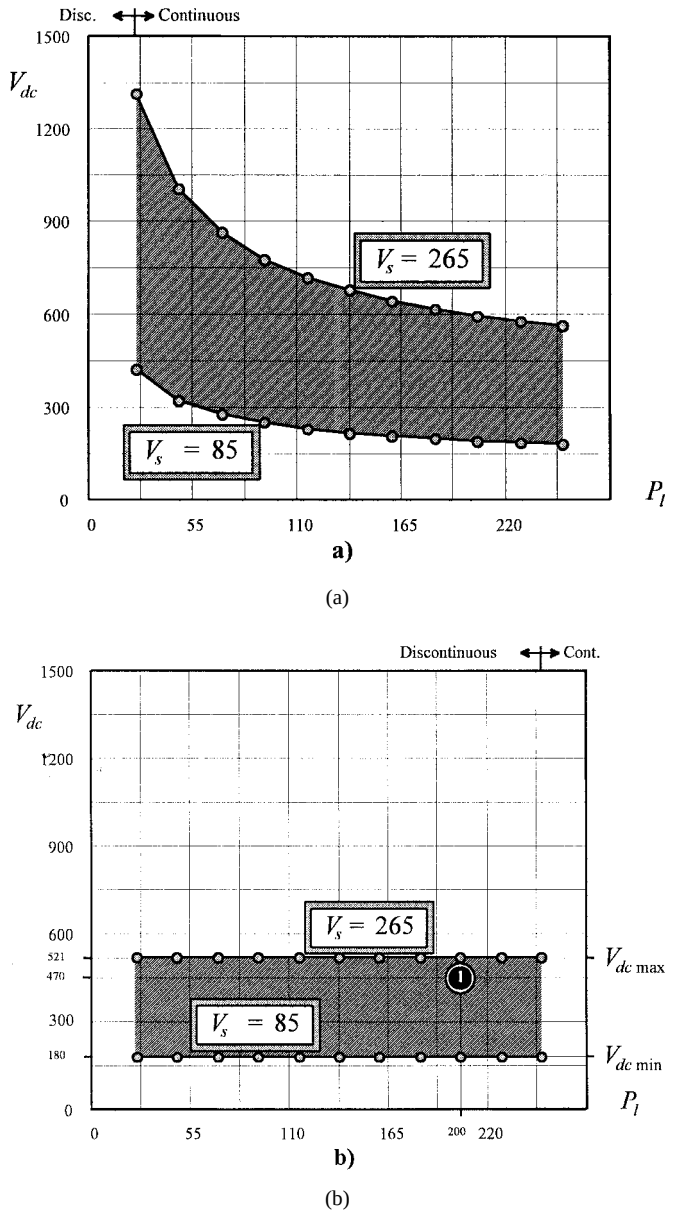


Fig. 5. Operating region of the power supply (shaded area). (a) Continuous mode (Case A in Table I). (b) Discontinuous mode (Case B in Table I). (①: simulated operating point in Fig. 2.)

hand, in discontinuous mode, that is, the proposed operating mode, the following expression is valid:

$$P_l = \frac{D^2}{4L_f f_{sw}} \left\{ \frac{V_{\rm dc}}{n_t} - V_l \right\} \frac{V_{\rm dc}}{n_t}. \tag{37}$$

Since the converter is considered lossless, the average supply power (32) equals the load average power (37). This yields in discontinuous mode

$$\left\{ \frac{V_{\rm dc}}{n_t} - V_l \right\} \frac{1}{n_t} = \sqrt{2} V_s \frac{L_f}{L_{\rm aux}} \frac{0.48\sqrt{2} V_s / V_{\rm dc}}{1 - 0.91\sqrt{2} V_s / V_{\rm dc}}. \tag{38}$$

The load power level P_l is not present in (38). This shows that only the supply voltage V_s defines the dc-link voltage $V_{\rm dc}$. The values of $V_{\rm dc}$ which satisfy (38) are plotted in Fig. 5(b). They correspond to the operating region of the power supply in discontinuous mode.

As expected, Fig. 5(b) shows that, in discontinuous mode, the dc-link voltage $V_{\rm dc}$ is independent of the load power level P_l. On the contrary, it depends upon both the load power level P_l and supply voltage V_s in continuous mode [Fig. 5(a)]. Moreover, at low power levels, the continuous operating mode may require an excessive dc-link voltage $V_{\rm dc}$ [Fig. 5(a)]. Therefore, to reduce the voltage stress across the dc-link capacitor, the proposed converter is recommended to operate in the discontinuous output current mode.

B. The Duty Cycle D and Performance Indexes Range

The duty cycle D and the total load inductor current conduction time $D + \Delta_l$ for the operating region are plotted in Fig. 6(a) and (b), respectively. It can be seen from Fig. 6(a) that the load power P_l can be effectively controlled by means of the duty cycle D. Fig. 6(a) also shows that the maximum duty cycle $D_{\rm max}$ is achieved at minimum supply voltage $V_{s\ \rm min}$ and maximum load power $P_{l\ \rm max}$. From Fig. 5(b), these conditions lead to minimum dc-link voltage. Fig. 6(b) confirms that these conditions are achieved in the load boundary condition $D + \Delta_l = 1$. Therefore, the assumptions used to determine the transformer turns ratio n_t and the auxiliary inductor $L_{\rm aux}$ expressions in Section III are thus confirmed.

Fig. 6(c) plots the dc-link voltage peak-to-peak ripple $\Delta V_{\rm dc}$. It can be seen that the maximum dc-link voltage ripple $\Delta V_{\rm dc\ max}$ is achieved at minimum supply voltage $V_{s\ \rm min}$ and maximum load power $P_{l\ \rm max}$. Therefore, the assumptions used to determine the expression for the minimum dc-link capacitor $C_{\rm dc}$ in Section III are, thus, confirmed. In this paper, the maximum dc voltage ripple has been limited to 1% ($\Delta V_{\rm dc\ max} = 5.21$ V) of the maximum dc-link voltage ($V_{\rm dc\ max} = 521$ V).

Finally, Fig. 6(d) depicts the load voltage ripple. It can be seen that the maximum load voltage ripple $\Delta V_{l\ \rm max}$ is achieved at minimum supply voltage $V_{s\ \rm min}$ and maximum load power $P_{l\ \rm max}$. Fig. 6(d) also confirms that the load voltage ripple $\Delta V_{l\ \rm max}$ is achieved at the load boundary condition. Therefore, the assumptions used to determine the expression for the minimum load capacitor C_f in Section III are also confirmed. In this paper, the dc voltage ripple at the boundary condition has been limited to 1% ($\Delta V_{l\ \rm max} = 480$ mV) of the load voltage ($V_l = 48$ V).

C. The Maximum Duty Cycle $D_{\rm max}$ Selection

Section III assumes that the maximum duty cycle $D_{\rm max}$ is a known parameter. The value is usually chosen large enough so that the peaks of the supply current are minimized. However, it will be shown that the maximum duty cycle $D_{\rm max}$ defines the maximum dc-link voltage $V_{\rm dc\ max}$ in Fig. 5(b), which restricts the maximum duty cycle $D_{\rm max}$.

Expression (38) is valid in any operating point of the power supply. According to Fig. 5(b), the maximum dc-link voltage $V_{\rm dc\ max}$ is achieved at maximum supply voltage $V_{s\ \rm max}$. Therefore, (38) can be written as

$$\frac{V_{\rm dc\ max}}{n_t^2} - \frac{V_l}{n_t} = \frac{L_f}{L_{\rm aux}} \frac{0.96 V_{s\ \rm min}^2 / V_{\rm dc\ max}}{L_{\rm aux} 1 - 0.91\sqrt{2} V_{s\ \rm min} / V_{\rm dc\ max}}. \tag{39}$$

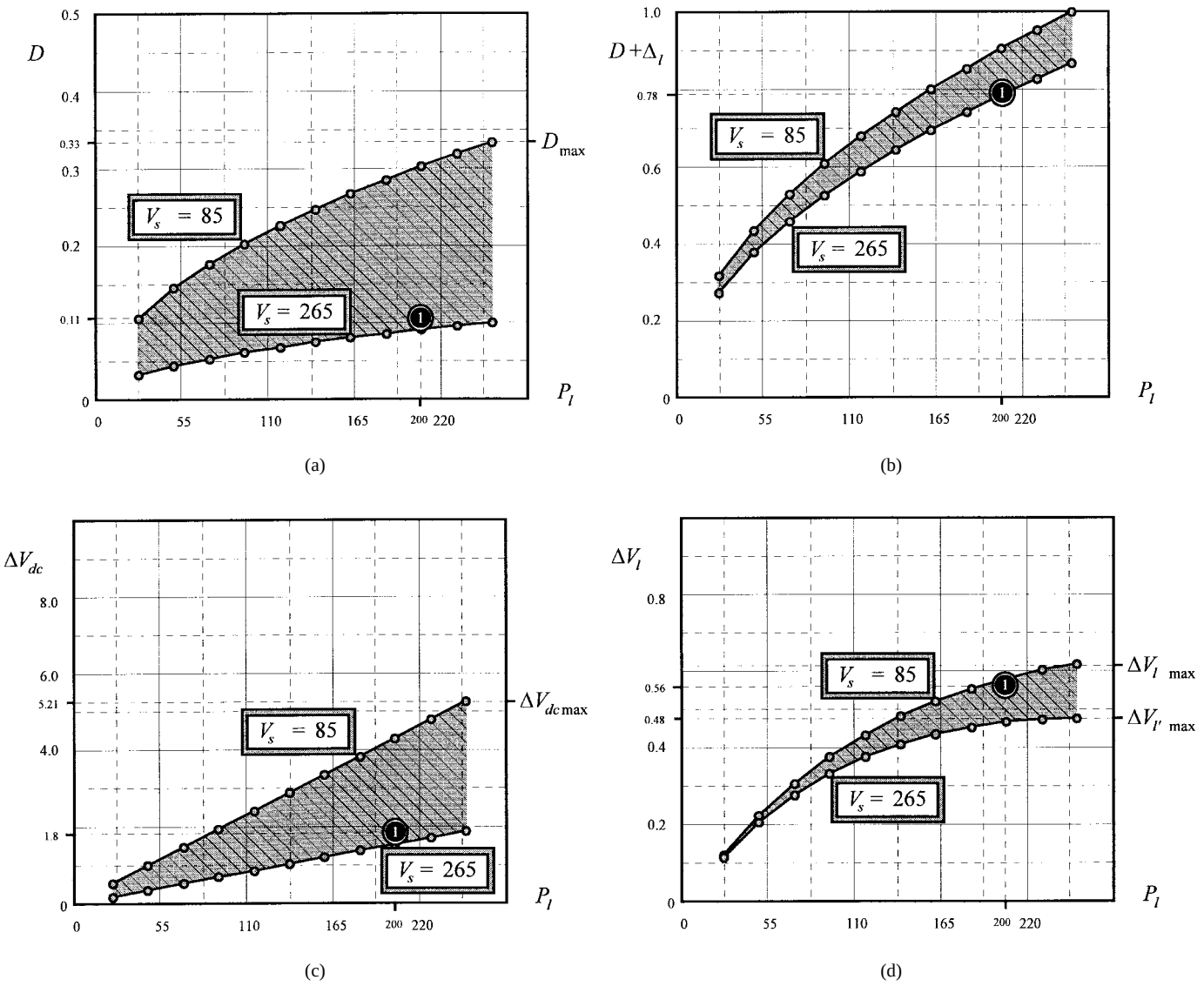


Fig. 6. Operating ranges of relevant variables and indexes of the power supply as a function of the load power. (a) Duty cycle. (b) Total load inductor current conduction time ($D + \Delta_l$). (c) Dc link voltage ripple. (d) Load voltage ripple. (① simulated operating point in Fig. 2.)

Replacing the turns ratio (13), auxiliary inductor (19), and load inductor (29) expressions into (39), the following expression is obtained:

$$1 - D_{\max}\left\{\frac{\sqrt{2}V_{s\,\min}}{V_{\mathrm{dc\,max}}} + 1\right\} = \frac{1}{\Psi_1}\frac{0.48\left(\dfrac{\sqrt{2}V_{s\,\max}}{V_{\mathrm{dc\,max}}}\right)^2}{1 - 0.91\dfrac{\sqrt{2}V_{s\,\max}}{V_{\mathrm{dc\,max}}}}. \tag{40}$$

The values of $V_{\mathrm{dc\,max}}$ and $D_{\max}$ that satisfy (40) are plotted in Fig. 7 for different supply voltage ranges. From Fig. 7, the following conclusions can be drawn: 1) the maximum dc-link voltage $V_{\mathrm{dc\,max}}$ does not depend upon the load voltage V_l and power level P_l and 2) for a given maximum dc-link voltage $V_{\mathrm{dc\,max}}$, the maximum duty cycle $D_{\max}$ can be selected upon the supply voltage range. In practical applications, the maximum dc-link voltage $V_{\mathrm{dc\,max}}$ is limited by the voltage of the MOSFET's. In this paper, the supply voltage ranges from 85 to 265 and 600 V MOSFET's are used; therefore, a maximum duty cycle $D_{\max}$ of 0.33 is selected (Fig. 7).

V. Experimental Verification

To verify the behavior and analysis of the proposed operating mode, a prototype power supply was built and tested in the laboratory. Table I shows the conditions of the tests and the component values; however, a higher switching frequency $f_{sw} = 128$ kHz was used. This allowed the use of smaller filtering components. Specifically, using (19) and (29), the auxiliary inductor and load filter inductor values are reduced to $L_{\mathrm{aux}} = 15\ \mu$H and $L_f = 12\ \mu$H, respectively. The capacitive components can also be further reduced. In this implementation, the dc-link capacitor and the load capacitor values are $C_{\mathrm{dc}} = 390\ \mu$F (27) and $C_f = 390\ \mu$F (31), respectively.

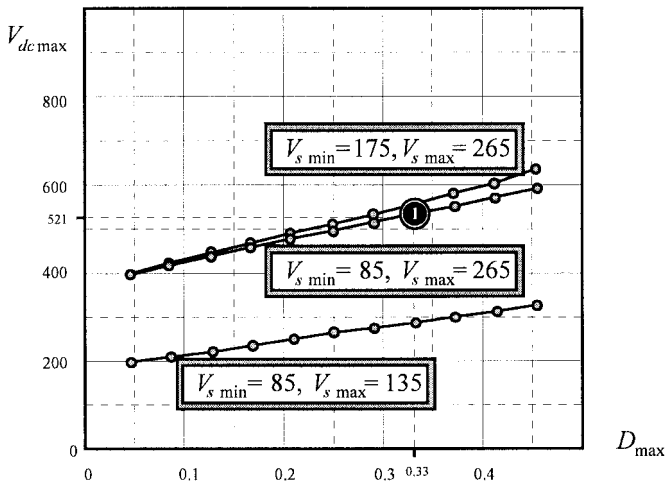


Fig. 7. Maximum dc-link voltage as a function of the maximum duty cycle for different supply voltage ranges. (①: chosen maximum duty cycle.)

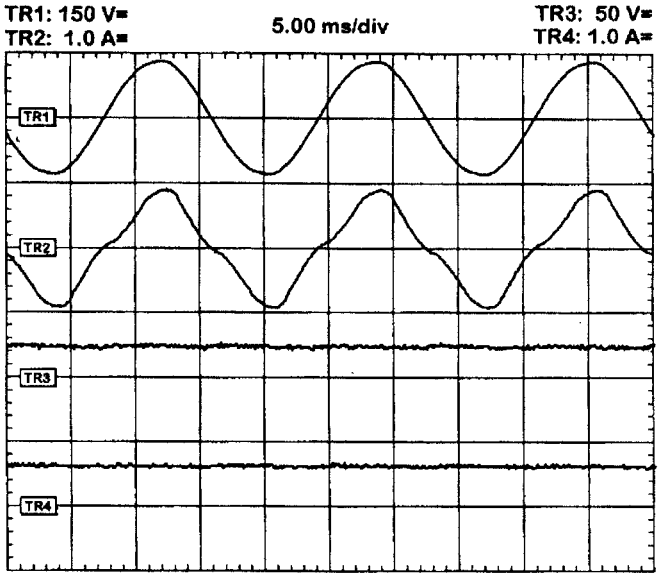


Fig. 8. AC mains and load experimental waveforms for $V_s = 90$ V, $P_l = 50$ W, and $f_{sw} = 128$ kHz. TR1: supply phase voltage (v_s). TR2: supply line current after filtering (i_s). TR3: load voltage (v_l). TR4: load current (i_l).

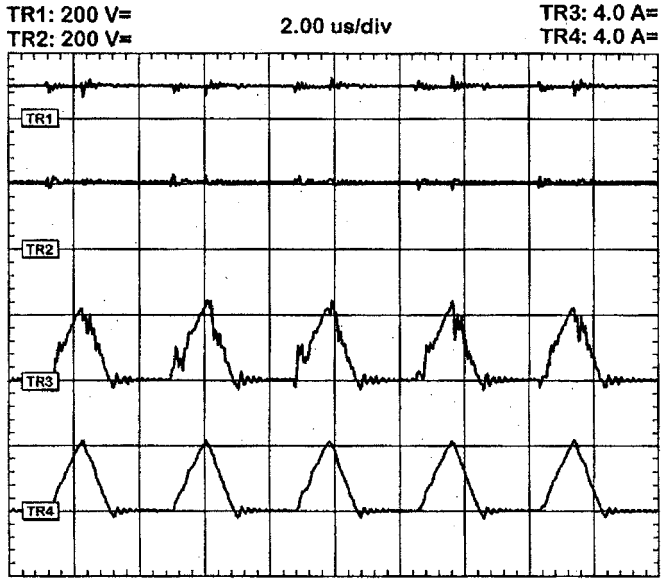


Fig. 9. Power supply experimental waveforms for $V_s = 90$ V, $P_l = 50$ W, and $f_{sw} = 128$ kHz. TR1: supply phase voltage (v_s). TR2: dc-link voltage ($v_{\rm dc}$). TR3: supply line current (i_s). TR4: auxiliary inductor current ($i_{L_{\rm aux}}$).

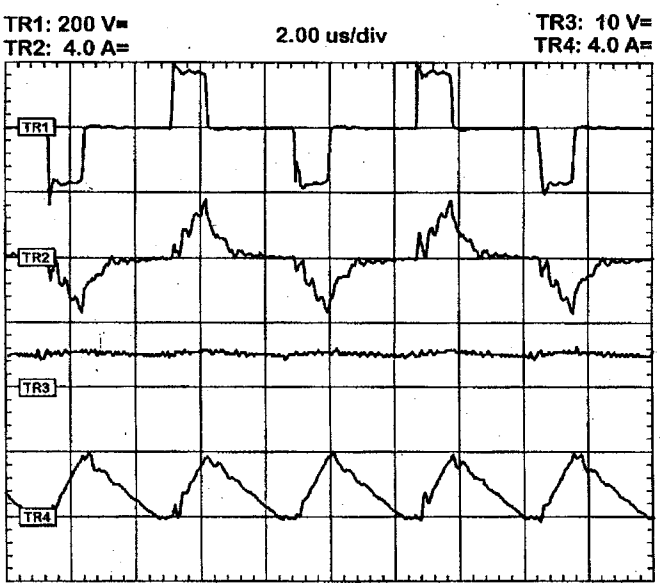


Fig. 10. Power supply experimental waveforms for $V_s = 90$ V, $P_l = 50$ W, and $f_{sw} = 128$ kHz. TR1: inverter ac voltage ($v_{\rm ac}$). TR2: inverter ac current ($i_{\rm ac}$). TR3: load voltage (v_l). TR4: load filter inductor current (i_{Lf}).

Fig. 8 shows the ac mains and load waveforms for $V_s = 90$ V and $P_l = 50$ W. These waveforms show that the input current after filtering (Fig. 8, TR2) is near sinusoidal and in phase with the supply phase voltage. Therefore, a near unity input power is achieved.

Figs. 9 and 10 show additional waveforms of the power supply. The corresponding simulated waveforms are shown in Fig. 3. The supply line current before filtering is shown in Fig. 9, TR3, which, neglecting the high-frequency oscillations, it corresponds, to the auxiliary inductor current (Fig. 9, TR4). It is evident from this figure that the input current operates in discontinuous mode. Fig. 10 shows that the inverter ac current (Fig. 10, TR2) is discontinuous. This comes from the fact that the supply current is discontinuous. Therefore, switches S_{g1} and S_{g4} are turned on at zero current. On the other hand, since the ac current remains positive after switches S_{g2} or S_{g3} are switched off, their turn-on is done at zero voltage. Both features contribute to reduced switching overall losses. The load filter inductive current waveform (Fig. 10, TR4) confirms the operation of the load stage at discontinuous current.

Fig. 11 shows the variation of the dc-link voltage $V_{\rm dc}$ as a function of the load power P_l. The tests were done at very low power, where the continuous load inductor current operating mode requires a high dc-link voltage [Fig. 5(a)]. It is evident from Fig. 11 that the dc-link voltage $V_{\rm dc}$ remains bounded and independent of the load power P_l. Finally,

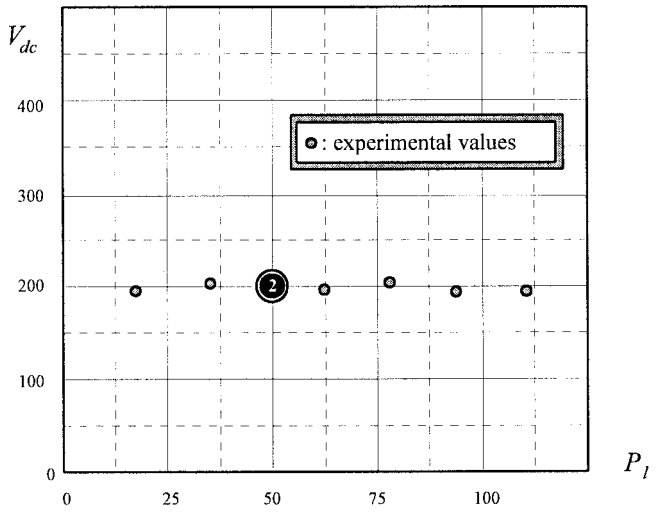


Fig. 11. DC-link voltage variation as a function of the load power for $V_s = 90$ V. ②: operating point in Figs. 8–10.

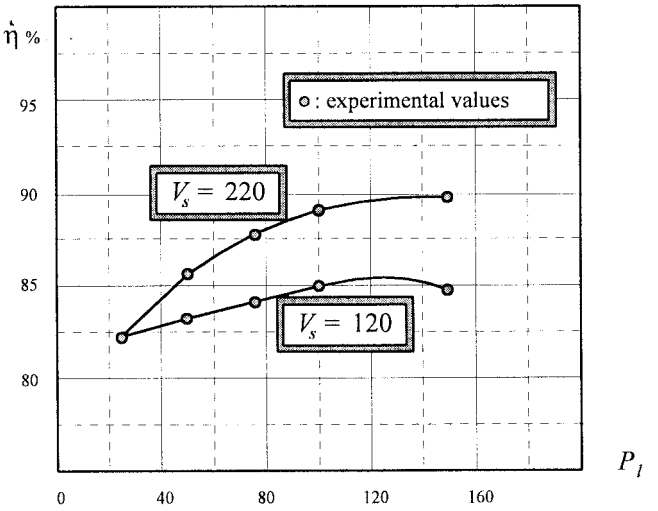


Fig. 12. DC power supply efficiency (η) as a function of the load power.

Fig. 12 shows efficiency tests for different load power levels and supply voltages. Although the power supply requires a transformer that includes a third winding, the power supply offers efficiency values near 90% as a result of the zero-voltage zero-current feature of the topology.

VI. Conclusions

A single-stage power-factor-corrected pulsewidth modulation converter with extended load power range has been presented. The topology is based on a zero-voltage zero-current-switched full-bridge (ZVZCS-FB) inverter. The steady-state analysis of the topology has shown that by operating the LC load filter in discontinuous mode, the dc-link voltage remains bounded and independent of the load voltage and power level. Therefore, the load power range can be further expanded, including the no-load operating condition. Experimental results have been included to prove the feasibility of the proposed operating mode.

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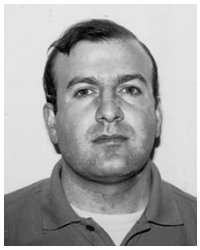

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